



This “A” Wor(l)d,
or 25 happy years in Newcastle
and 100 Technical Reports on
async.org.uk

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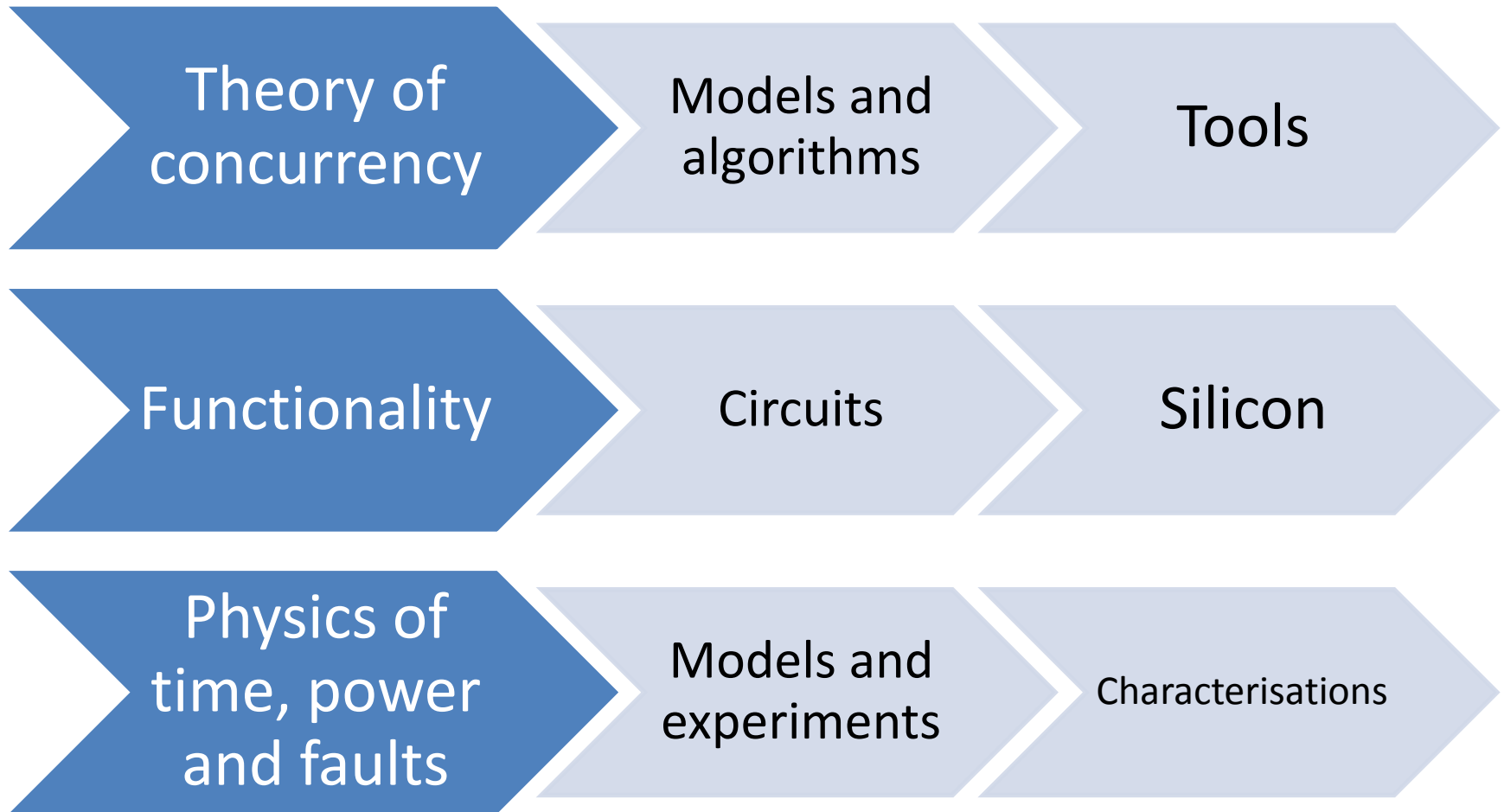
Outline

- **There is no Outline today!!!**

How it all began ...

- Prior to that:
 - David Kinniment's research on async processor designs and metastability and synchronisers in the 60s & 70s (Manchester)
 - My research on async design, models, interfaces in the 80s (St. Petersburg)
 - 1984-85 joint work (with Harry Whitfield, Albert Koelmans and Martin McLaughlin) on CAD for async (Newcastle) plus interactions with Brian Randell and Maciej Koutny on concurrency and dependability

Three main research threads



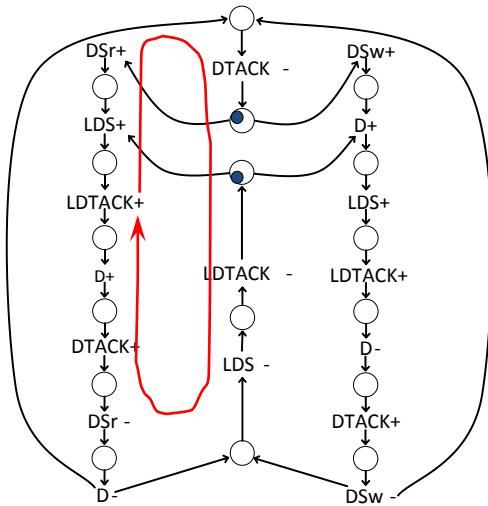
The key element for success

- Work of a team where all aspects of talent have a chance to develop and flourish
- The team – both locally (Newcastle) and globally (worldwide)
- Async research is a wonderful area which combines the three main threads and different people can exploit the three main categories of strengths:
 - Computer programming
 - Electronic (Circuits and Systems) design
 - Analytical

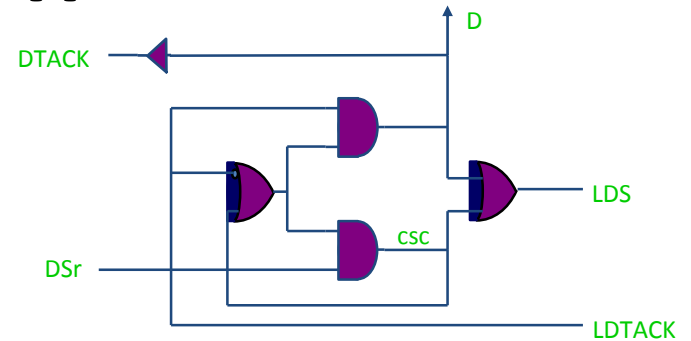
1990s: Logic Synthesis of Asynchronous Control

- Formalisation of STGs and relation to state-based models; theory, models and tools for async controller synthesis, async processor prototyping
- Projects: ASAP, ASTI, ACiD-WG
- People: Jordi Cortadella, Luciano Lavagno, Alex Kondratyev, Mike Kishinevsky, Alexander Taubin, Albert Koelmans, Alexei Petrov, Alex Semenov, Enric Pastor, Lee Lloyd, Marta Pietkiewicz-Koutny
- Some highlights: synthesis flow, monotonic cover, CSC solving, regions for async, Or-causality, relative-timing ('lazy' approach), unfolding-based verification (incl. nets with read-arcs), tool Petrify; application to Molnar's counterflow pipeline design

Petrify flow

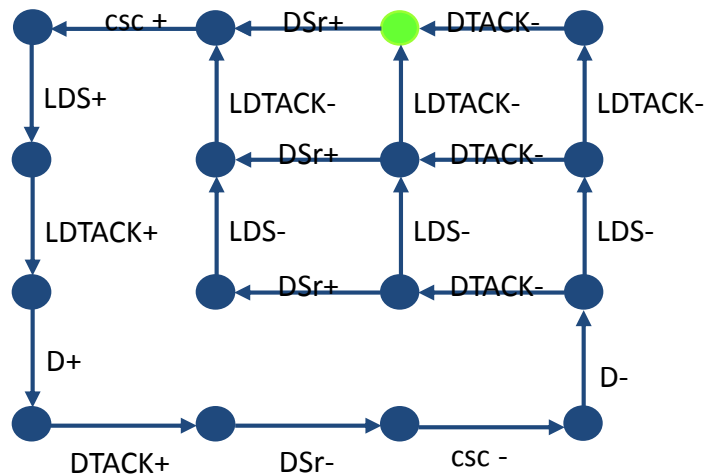


synthesis



Logic asynchronous circuit
(for Read Cycle)

Read Cycle State Graph (VME bus)



Boolean equations:

$$LDS = D \vee csc$$

$$DTACK = D$$

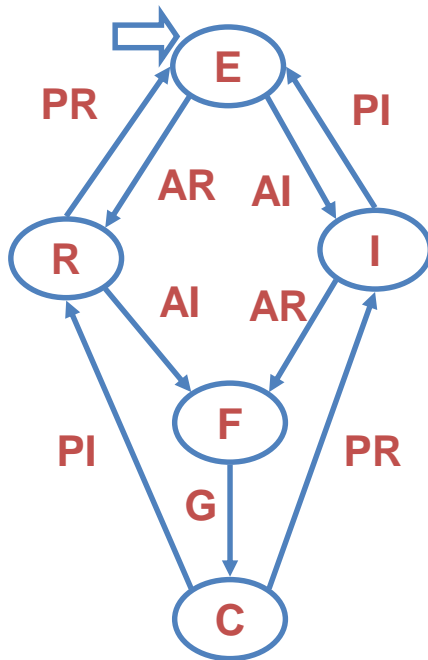
$$D = LDTACK$$

$$csc = DSr$$

Complete State Coding (CSC)

Example: counterflow pipeline

Molnar's 5-state TS:

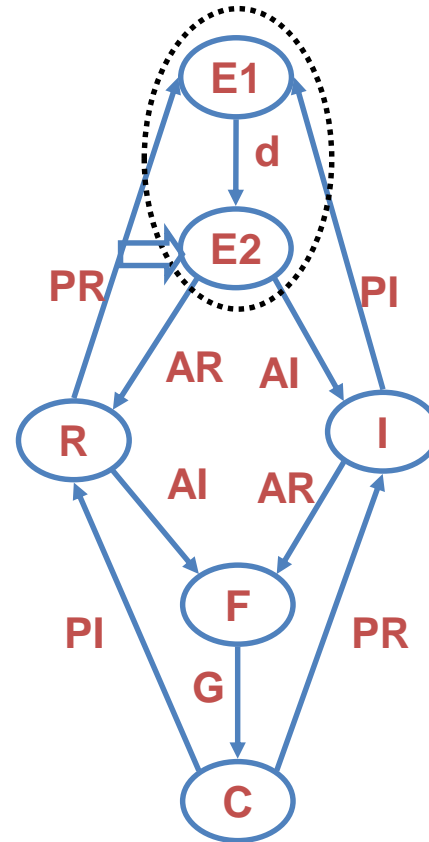
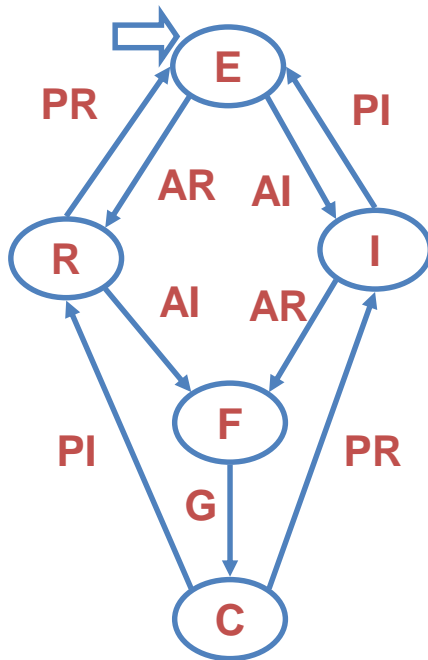


Solution:

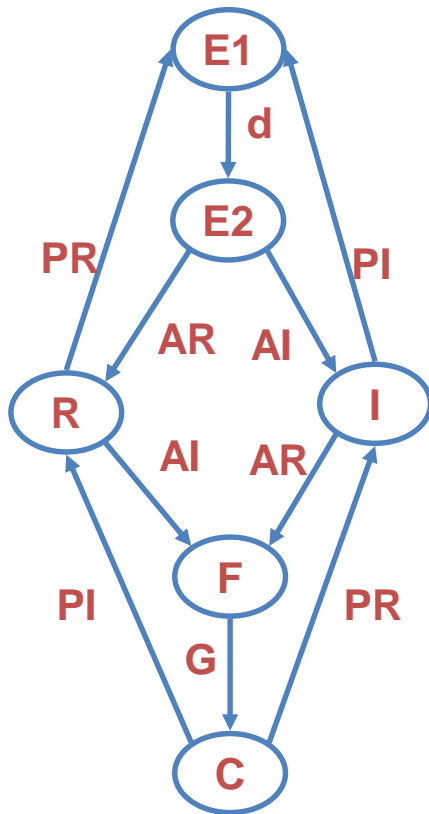
**Split a state (E) and insert
a silent action (d),
preserving behavioural
(observational)
equivalence**

Example: counterflow pipeline

Molnar's 5-state TS:



Example: counterflow pipeline



Semi-elementary TS



Minimal set of regions:

$r1 = \{E1, E2, I\} \leftarrow \text{pre}(AR), \text{post}(PR)$

$r2 = \{E1, E2, R\} \leftarrow \text{pre}(AI), \text{post}(PI), \text{co}(d)$

$r3 = \{R, F, C\} \leftarrow \text{pre}(PR), \text{post}(AR), \text{co}(G)$

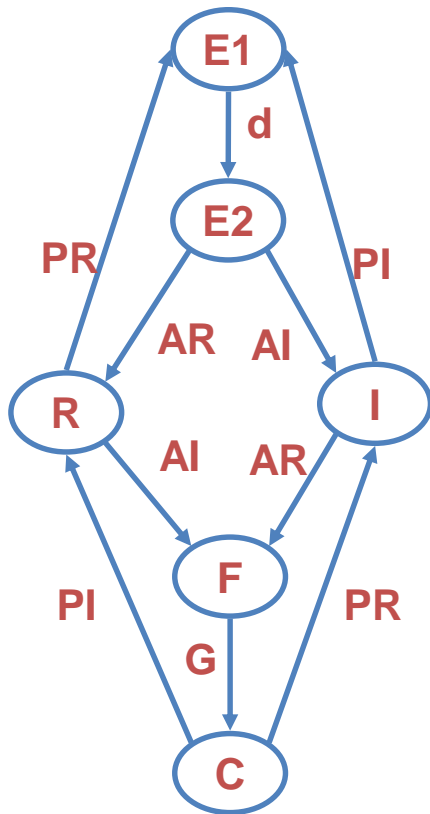
$r4 = \{I, F, C\} \leftarrow \text{pre}(PI), \text{post}(AI)$

$r5 = \{E2, I, C\} \leftarrow \text{pre}(PI, AR), \text{post}(G, d)$

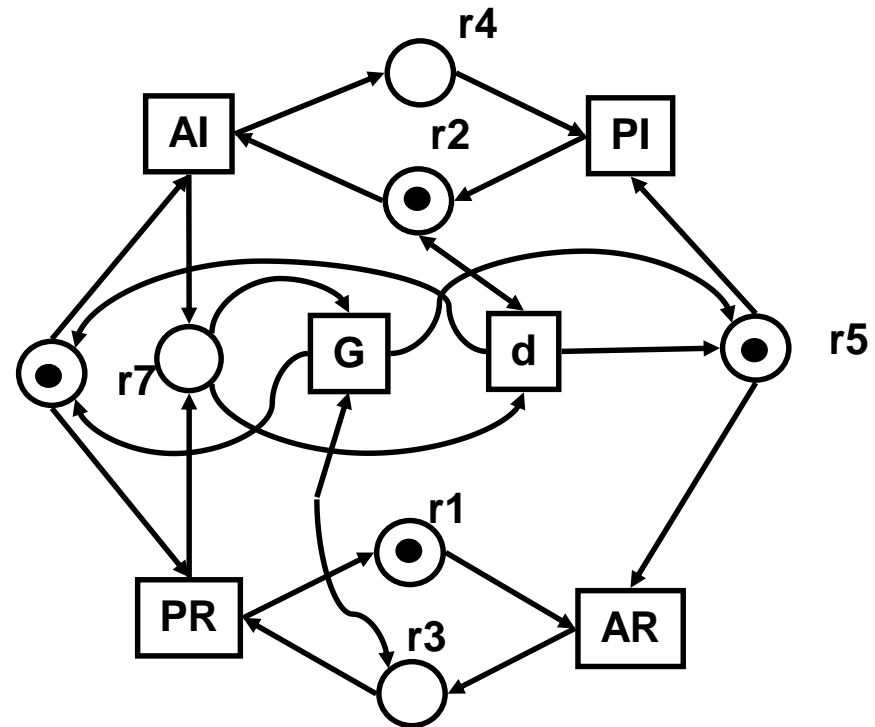
$r6 = \{E2, R, C\} \leftarrow \text{pre}(PR, AI), \text{post}(G, d)$

$r7 = \{E1, I, F\} \leftarrow \text{pre}(G, d), \text{post}(PR, AI)$

Example: counterflow pipeline

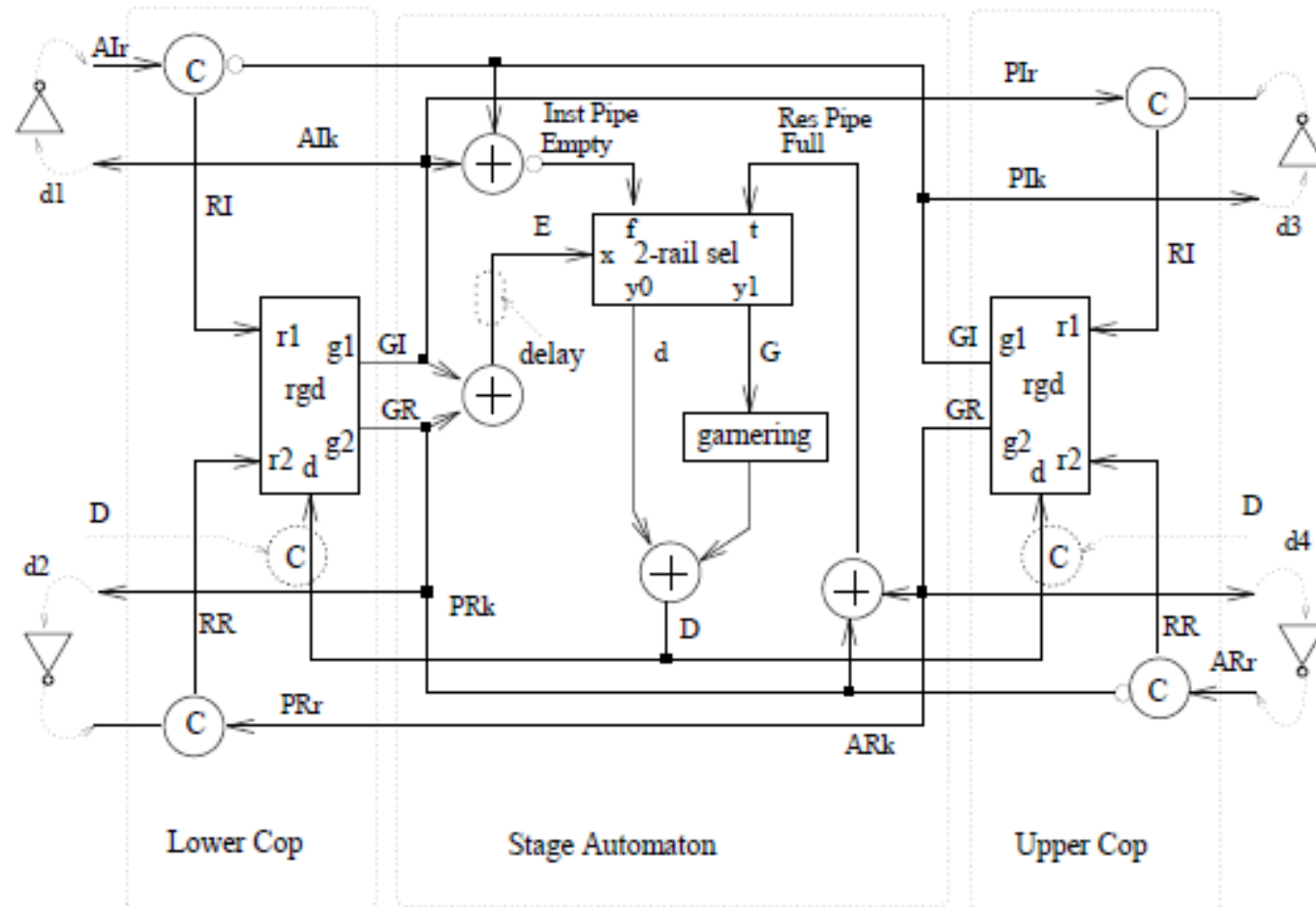


Semi-elementary TS



Semi-elementary Petri net

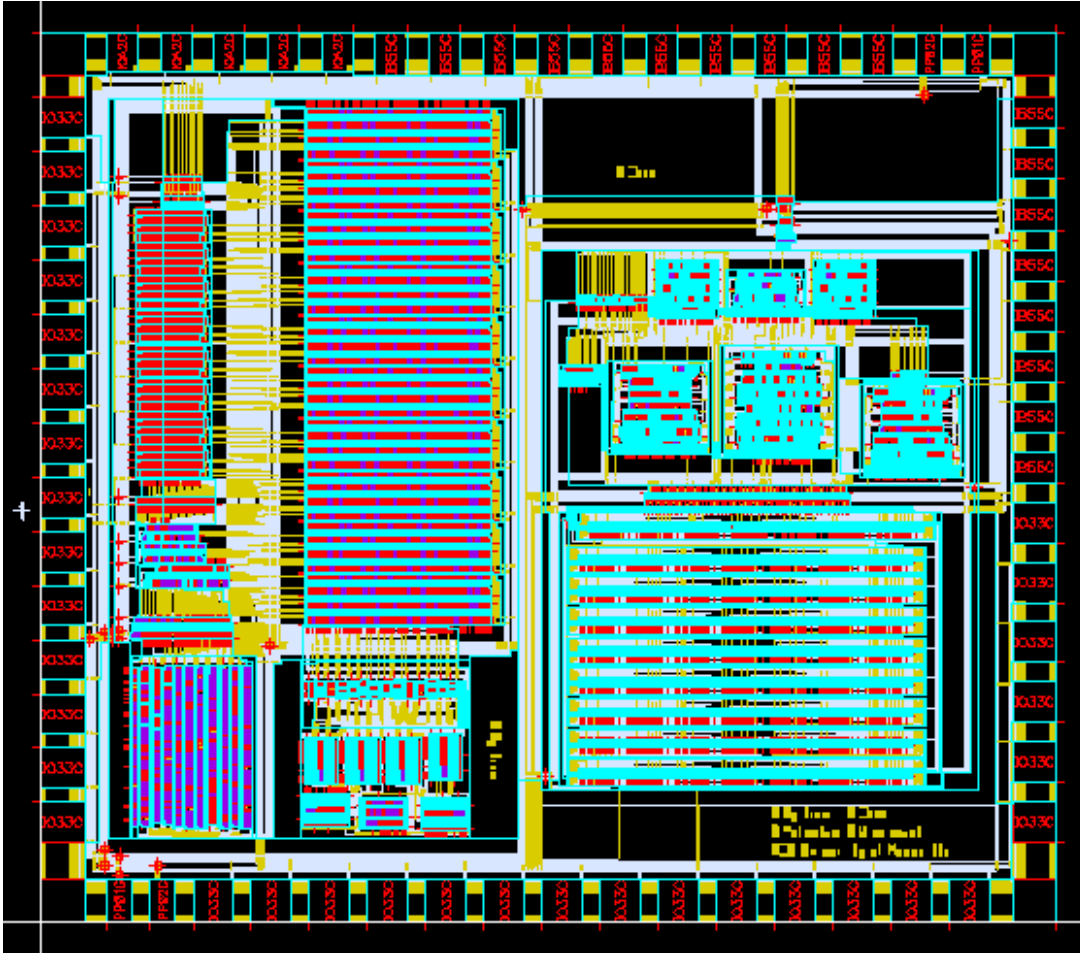
CFPP Implementation



1990s: Arbiter design

- Design of circuits with internal conflicts, all kinds of arbiters, modelling and analysis of arbiters asynchronous communication mechanisms
- Projects: HADES
- Highlights: method for factorising mutexes, new priority arbiters, 3 and 4 slot ACMs with mutexes
- People: David Kinniment, Fei Xia, Alex Bystrov, Delong Shang, Ian Clark, Bo Gao, Isi Mitrani, Tony Davies, Hugo Simpson and Eric Campbell (MBDA)
- First VLSI chip – HADIC (0.6um CMOS, Europractice)

HADIC: Our first Newcastle's asynchronous chip

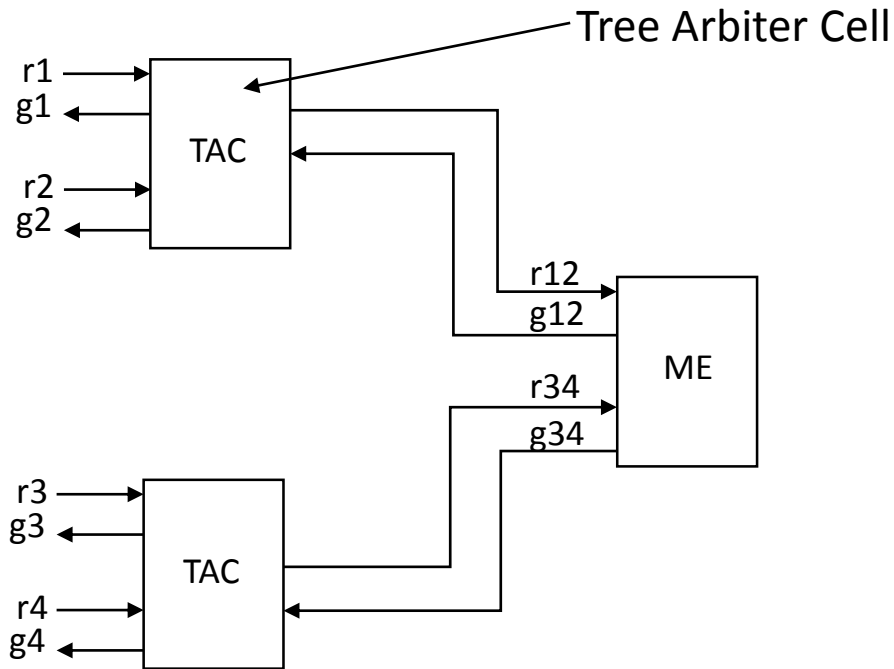


Designed using
Europractice
tools
On a SUN
w/station called
Sadko

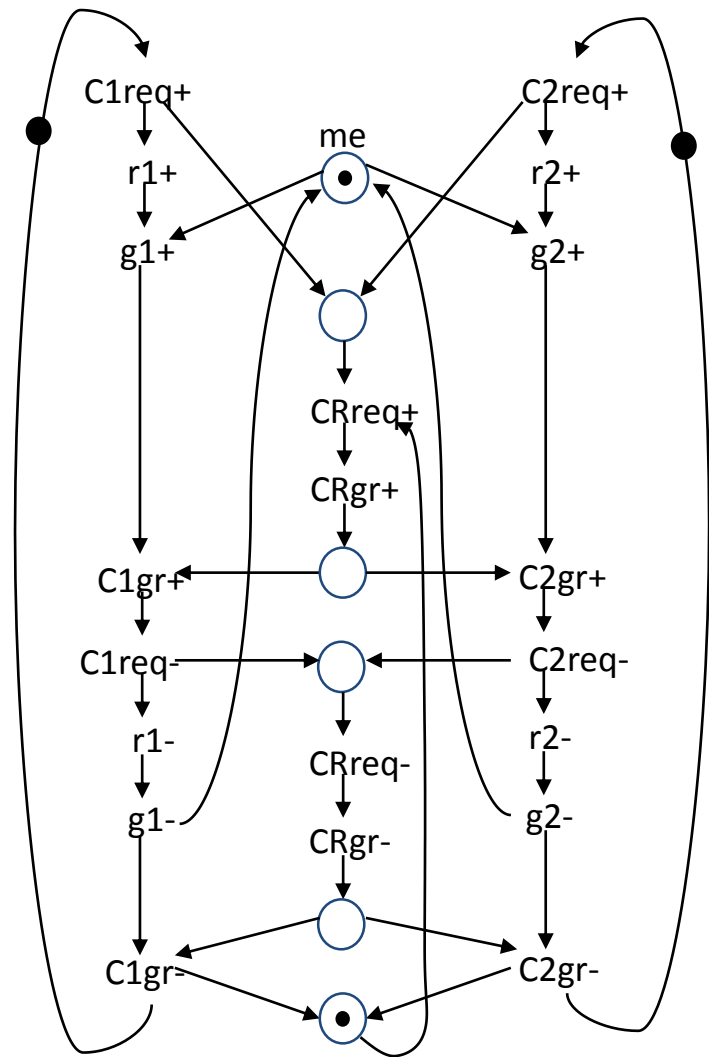
What HADIC had

- a **three-way ordered arbiter** comprising a three-way mutex element, based on a three-stable FF
- a **one-hot pipeline FIFO buffer**, and a request mask circuit, to demonstrate the effect of request-ordering in avoiding secondary metastability effects discussed,
- an **eight-way ordered arbiter with a low-latency tree arbiter** and a low-latency cyclic FIFO buffer, to demonstrate the role of low latency techniques in ordered arbitration with large numbers of channels,
- an **eight-way static priority arbiter** with a non-conventional (non-topological) priority allocation mapping to demonstrate the effect of static prioritisation defined as an arbitrary function,
- an **eight-way dynamic priority arbiter** with four priority levels (the priority data encoded in dual rail code) to study the variations of arbiter latency against different conditions of issuing prioritised requests and effects of early control signal propagation in the priority logic with a tree structure,
- an **eight-way token ring arbiter** with a one-level cascaded buffer, to study the effects of improved done-to-grant and practical fairness via buffering,
- a **comparator with a latch for an A/D converter**, to study the metastability effects in value/time domains,
- an **on-chip tester, for arbiters and asynchronous communication mechanisms**, containing a number of original circuits to experiment with system-on-chip testing.

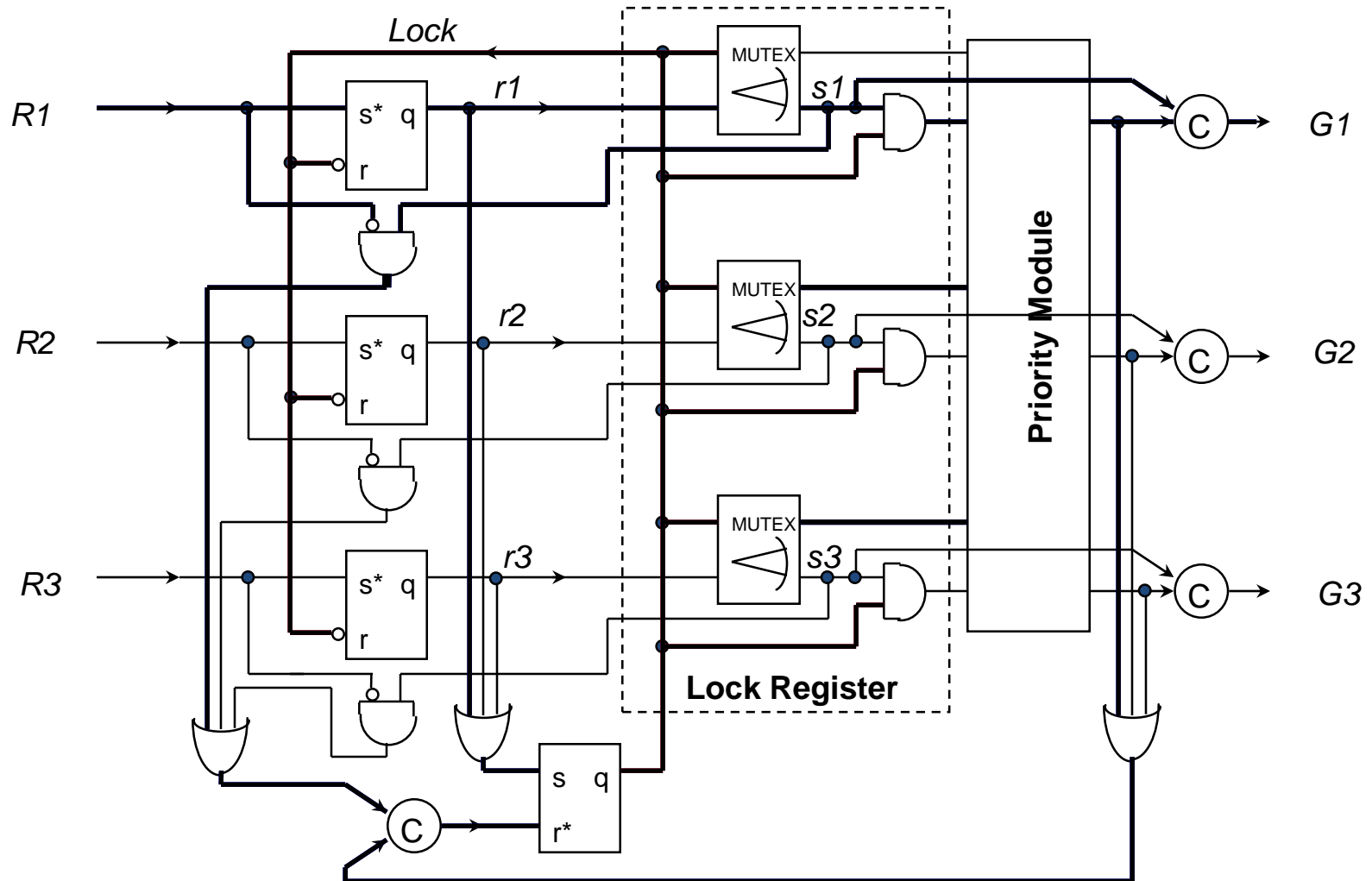
Example: Multiway Arbiters (tree)



4-way arbiter built as a cascade arbiter with OR-causal request propagation



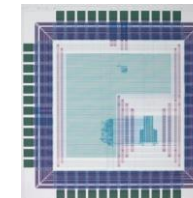
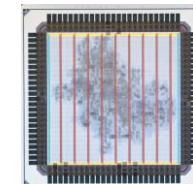
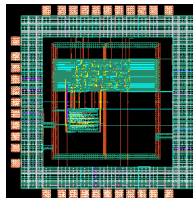
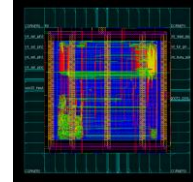
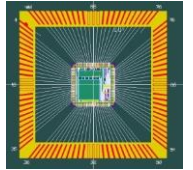
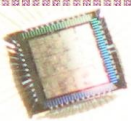
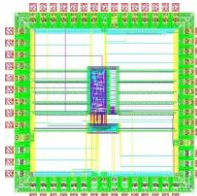
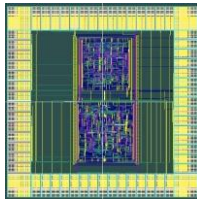
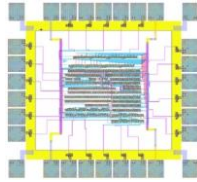
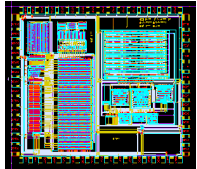
Example: static priority arbiter





Newcastle Async Chip Designs

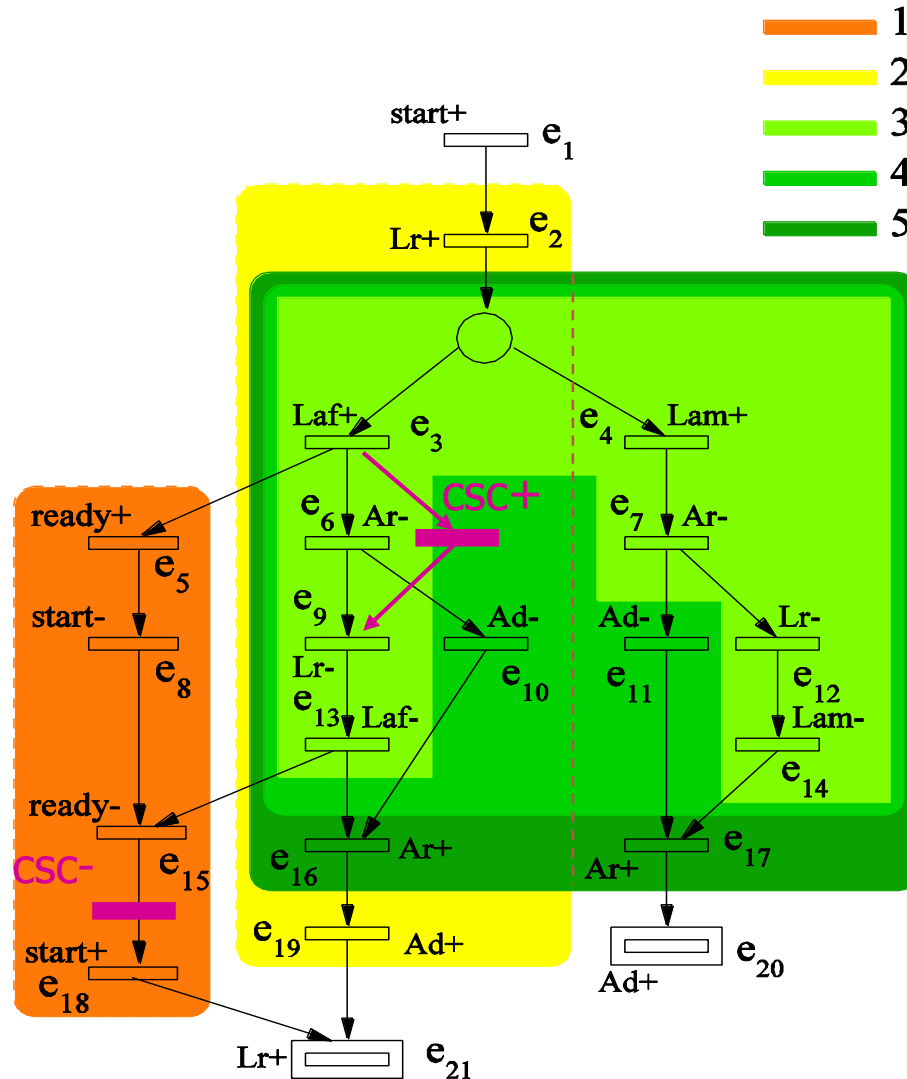
- **Arbitration:** HADIC1 (2000, CMOS 0.6 μ m) – asynchronous arbiters, ADC, Async communication mechanism
- **Time measurement:** TMC (2003, CMOS 0.2 μ m, collab. with Sun) time amplifier and time-to-digital converter
- **Synchronization:** SYRINGE1 (2006, UMC 0.18 μ m), SYRINGE2 (2008, UMC, 0.13 μ m) metastability measurement, robust synchronizer
- **Security:** SCREEN1 (2005, AMS 0.35 μ m), SCREEN2 (2006, AMS 0.18 μ m) AES cores with power balancing; SURE (2008, UMC 0.13 μ m), Galois Encoded Logic, Script1 &2 (2010, TSMC 90nm)
- **Networks on Chip:** NEGUS1 (2007, UMC 0.13 μ m), phase-encoding signalling, NeuroNOC (2009, TSMC 90nm) reconfigurable neural network, 3D-chip (2011, MIT Lincoln Labs, 150nm with TSVs)
- **Energy harvesting:** Holistic1 (2011, UMC 90nm), self-timed SRAM, Holistic 2 (2012, UMC 0.18 μ m), reference free voltage sensor
- **Power proportionality:** Async 8051 (2013, STM CMP 0.13 μ m)
- **SAVVIE and A4A chips:** to be reported



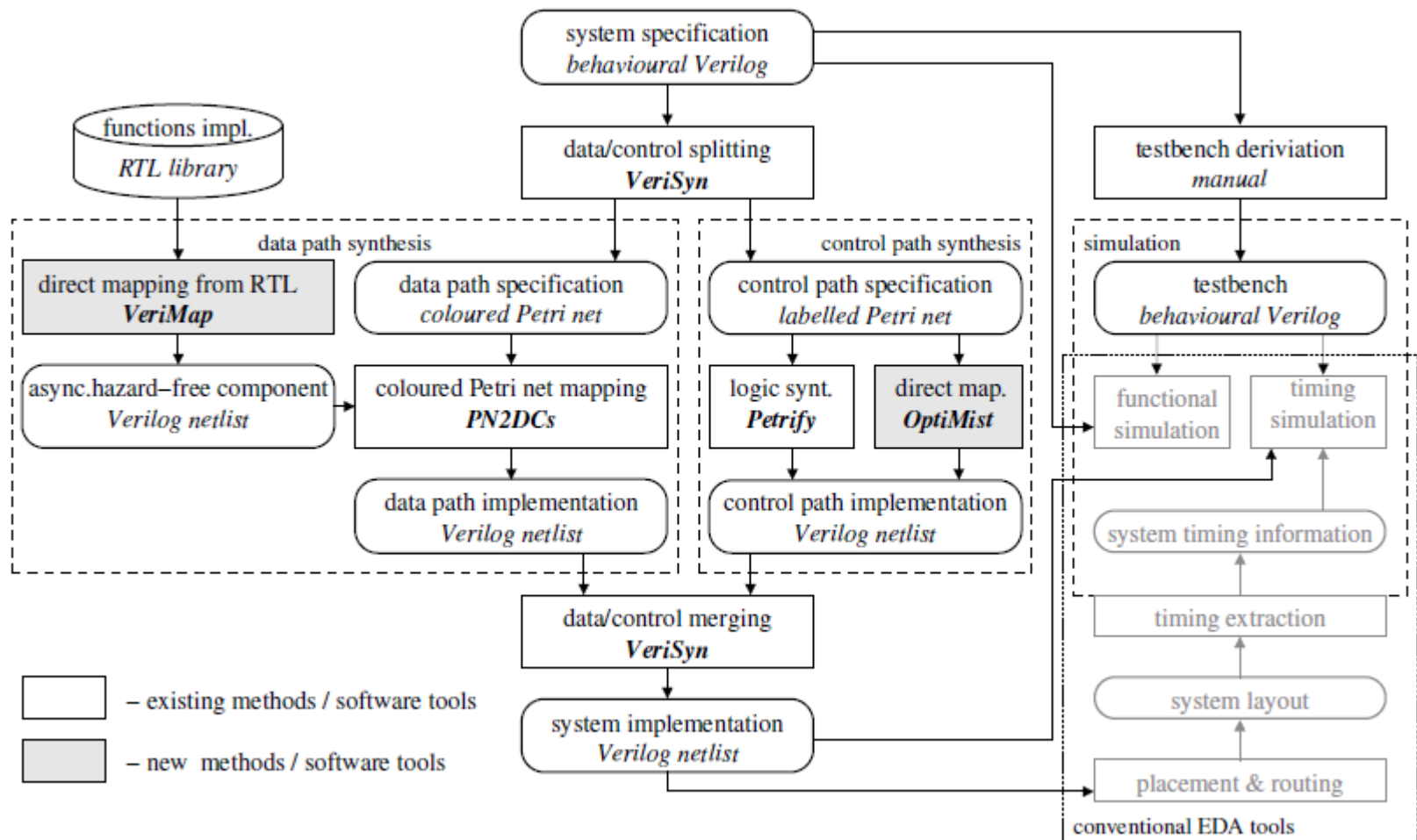
2000-2005: Synthesis and Testing

- Synthesis line: visualisation, unfolding-based synthesis, direct synthesis, negative gate synthesis, generalised OR-causality; regions, ACM synthesis
- Projects: BREACH, MOVIE, BESST, STELLA
- People: Maciej Koutny, Agnes Madalinski, Victor Khomenko, Danil Sokolov, Frank Burns, Deepali Koppad, Nikolai Starodoubtsev, Josep Carmona, Fei Hao, Kyller Gorgonyo
- Highlights: Core maps for visualization, Tracker-Bouncer for direct mapping, Lots of Tools: ConfRes, PUNF/MPSAT, Verisyn, Optimist, PN2DCs; application of direct mapping to S. Furber's duplex interface design; online testing for async protocols; generalised regions synthesis

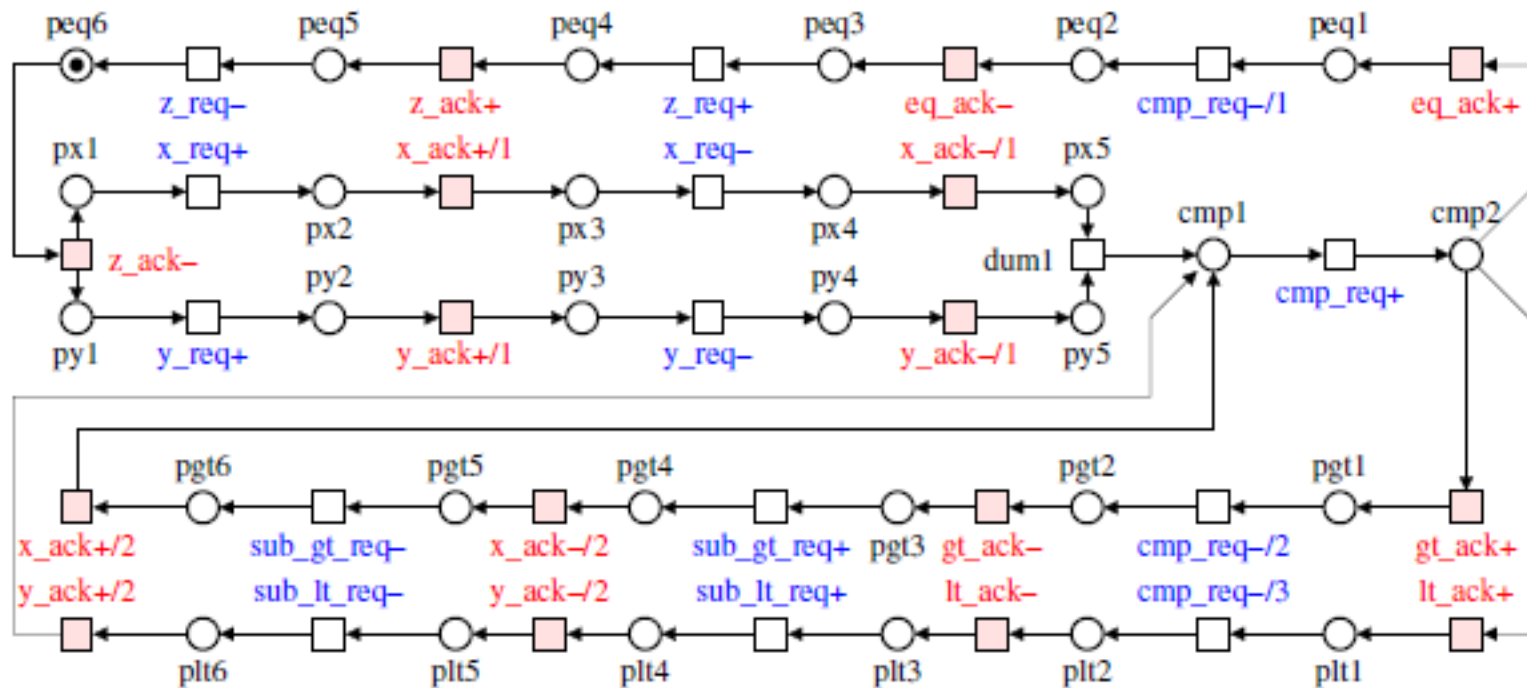
CSC Core visualisation using unfoldings



BESST Design Flow

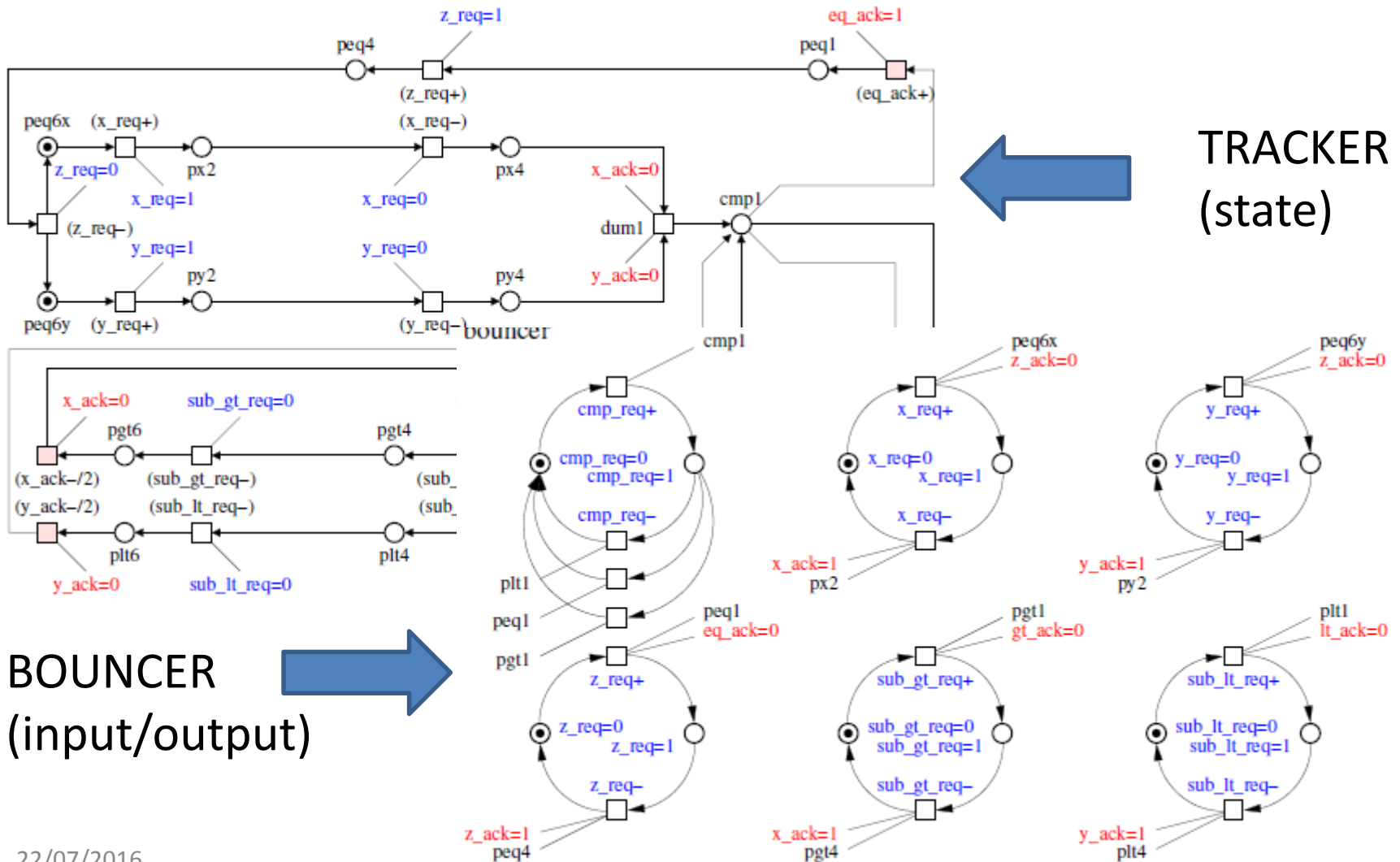


Example: GCD using Optimist flow

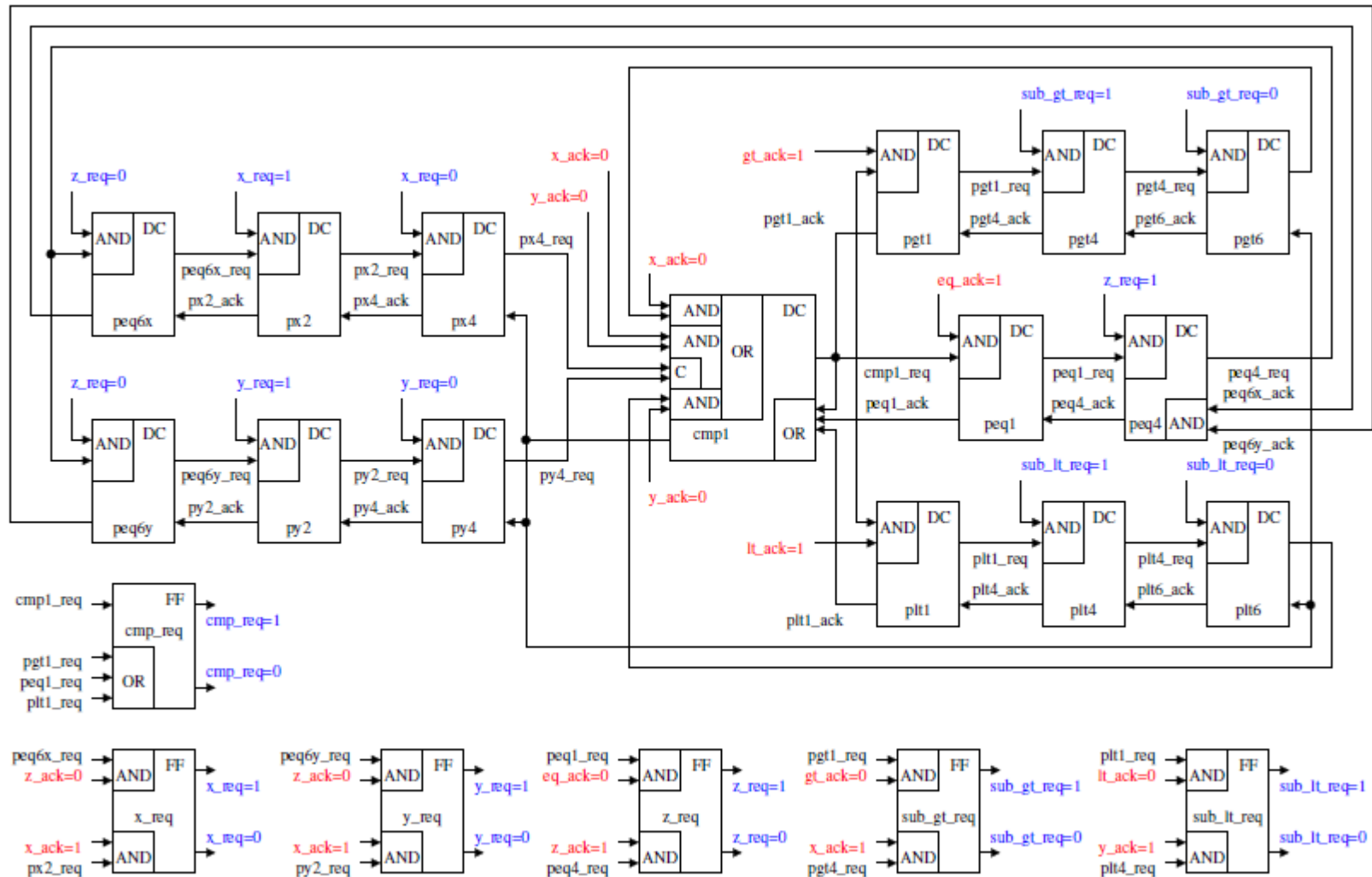


Range of Optimisations for latency and size could be applied

Example: GCD using Optimist



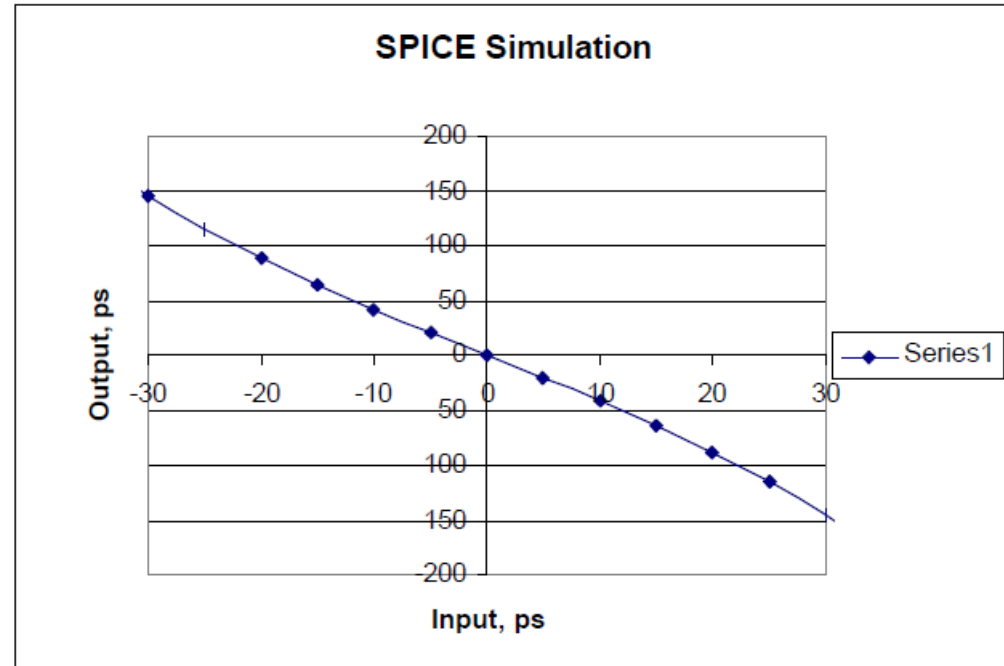
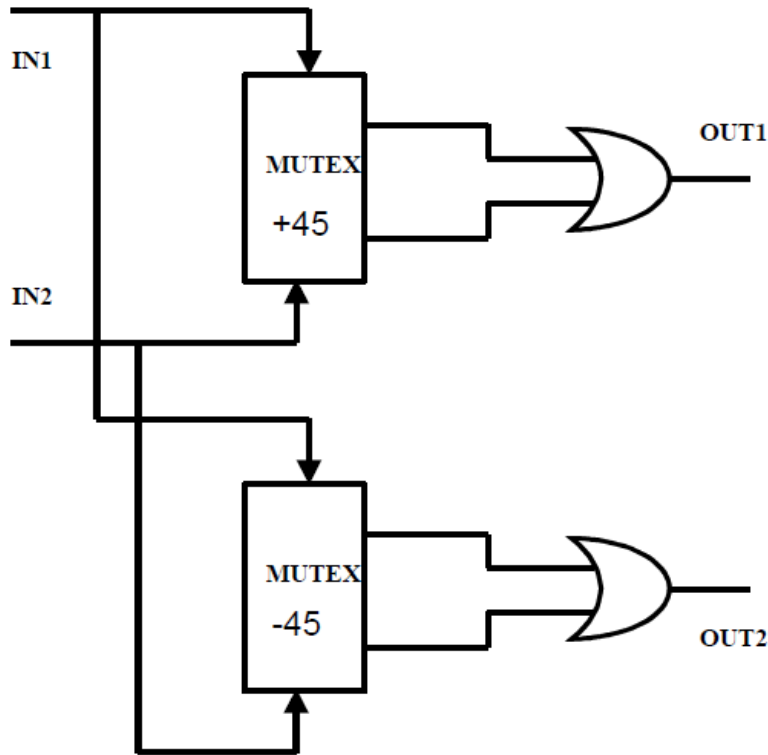
Direct mapping: David cell circuit



2000-2010: Metastability and Event Processing

- Synchronisation, time to digital conversion, time amplification, robust synchronization, speculative synchronization, dynamic systems models of analogue circuits
- Projects: COHERENT, STEP, SYRINGE, RelCel
- People: Gordon Russell, Graeme Chester, Oleg Maevsky, Amir Abbas, Nikos Minas, Keith Heron, Jun Zhou, Fei Hao, Yuan Chen, Stan Golubcova, Ghaith Tarawneh, Ioannis Syranidis, Ahmed Alahmadi, Mohammed Alshaikh, James Guido; collaboration with Charles Dike (Intel), Ian Jones (Sun/Oracle) Marc Renaudin (Grenoble)
- Highlights: Metastability physical measurements, RNG, TD converters, time amplifier, FPGA synchronisers, speculative synchronizers; reconfigurable synchronizers, soft arbiters; Several Chips (via Europractice and Sun)

Time difference amplifier

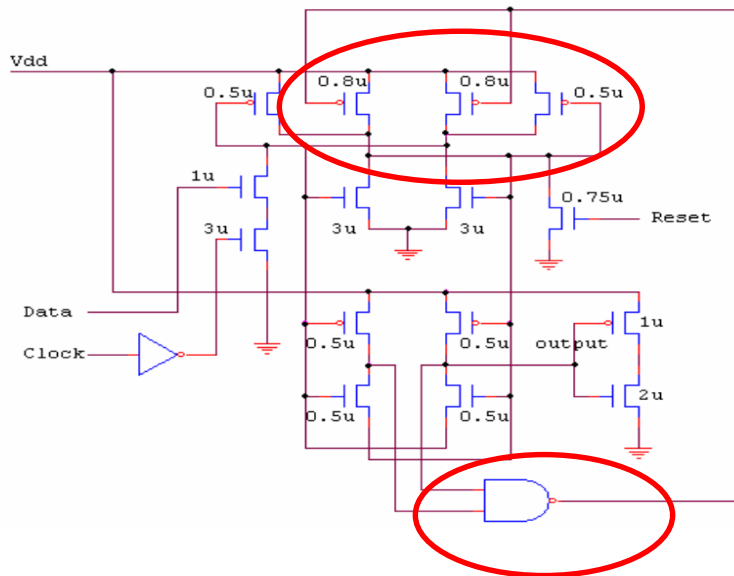


$$\Delta_{out} = \tau \cdot \ln(45 + \Delta_{in}) - \tau \cdot \ln(45 - \Delta_{in})$$

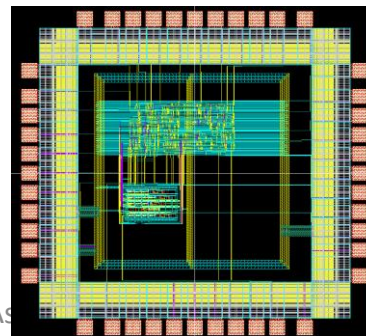
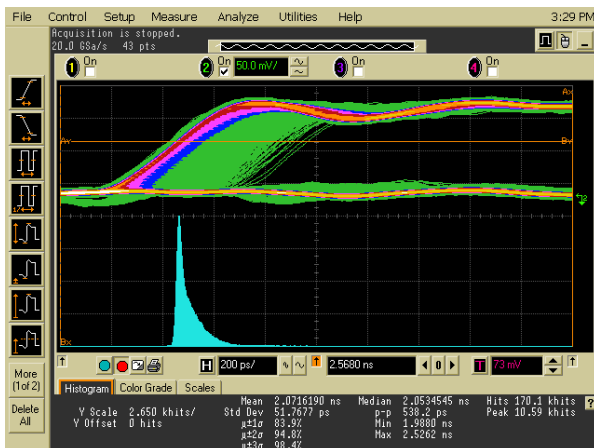
Was used as the first cascade of time2digital converter

Robust synchronizer

Dynamic feedback control

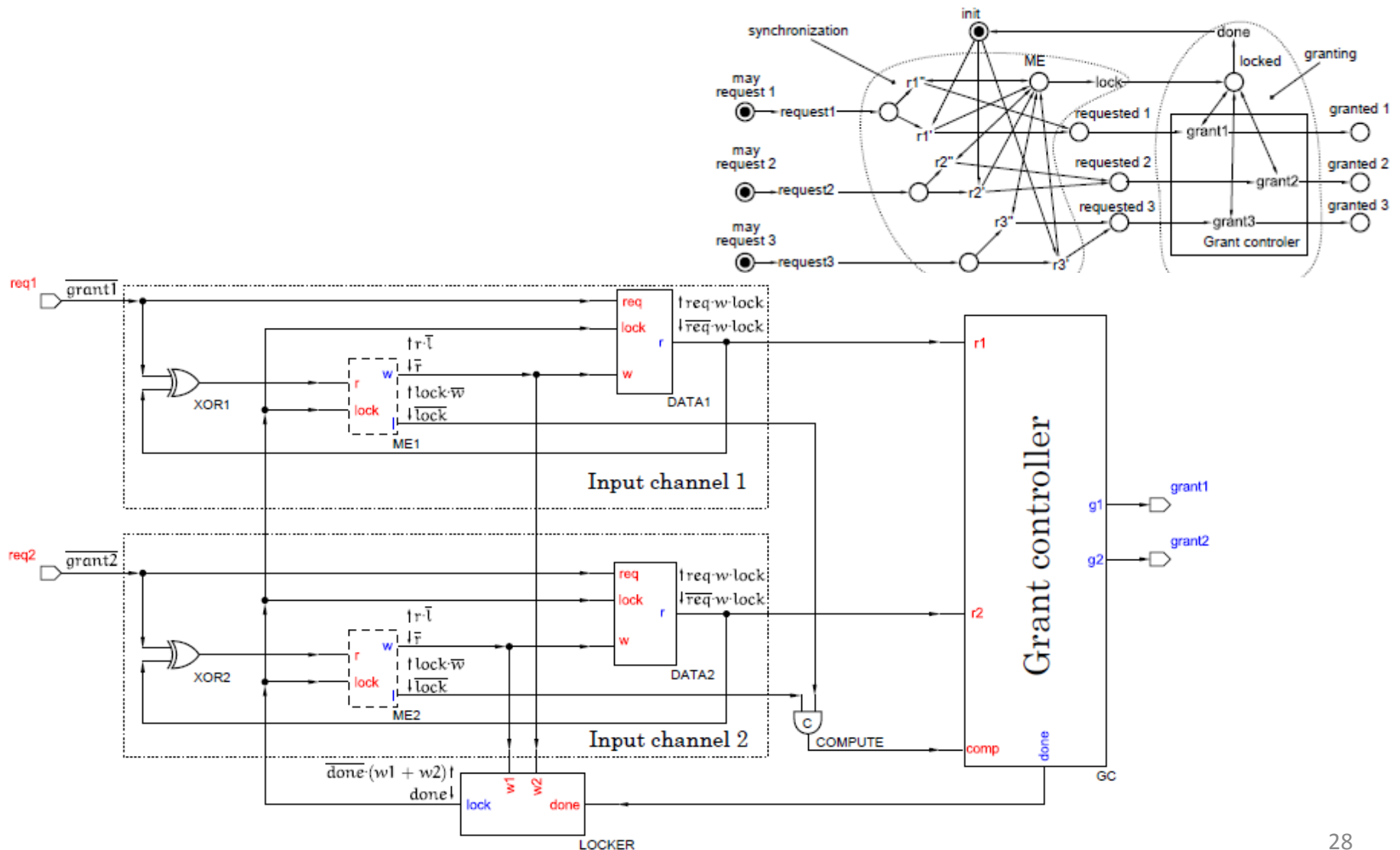


Vdd(v)	Measurement Results (ps)			
	Jamb Latch B		Robust Synchronizer	
	>10 ⁻¹⁴ s	<10 ⁻¹⁴ s	>10 ⁻¹⁴ s	<10 ⁻¹⁴ s
1.8	19.44	35.55	15.27	34.92
1.7	21.75	37.29	16.53	35.76
1.6	25.64	40.93	19.38	38.25
1.5	28.77	52.36	20.29	43.07
1.4	36.22	66.17	23.75	50.36
1.35	45.43	75.35	28.51	58.19



τ (metastability
time constant) vs
Vdd

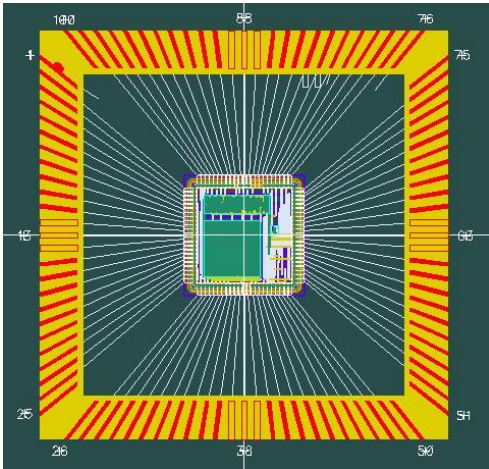
Multiway arbiters: general approach



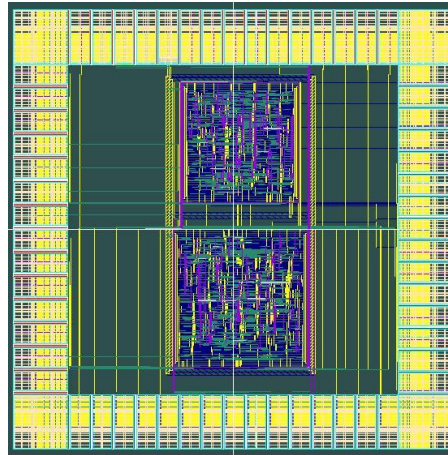
2004-2009: Security

- Asynchronous circuits for power-attack resistance, mixed radix synthesis
- Projects: SCREEN, SURE, STRIP
- People: Julian Murphy, Ashur Rafiev, Atmel people (Ewart Grey, Russell Hobson, Steve Pickles)
- Highlights: Automatic translation from single to dual rail; Tools: Verimap; RMMixed; Many Chips: SCREEN1/2, SURE, STRIP1/2

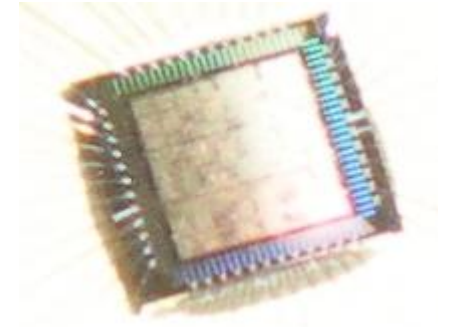
Some Security Chips



SCREEN1: AES
encryption core design
using alternating spacer
dual-rail signalling for
power balancing
(generated from
synchronous RTL using
in-house tool VeriMap)

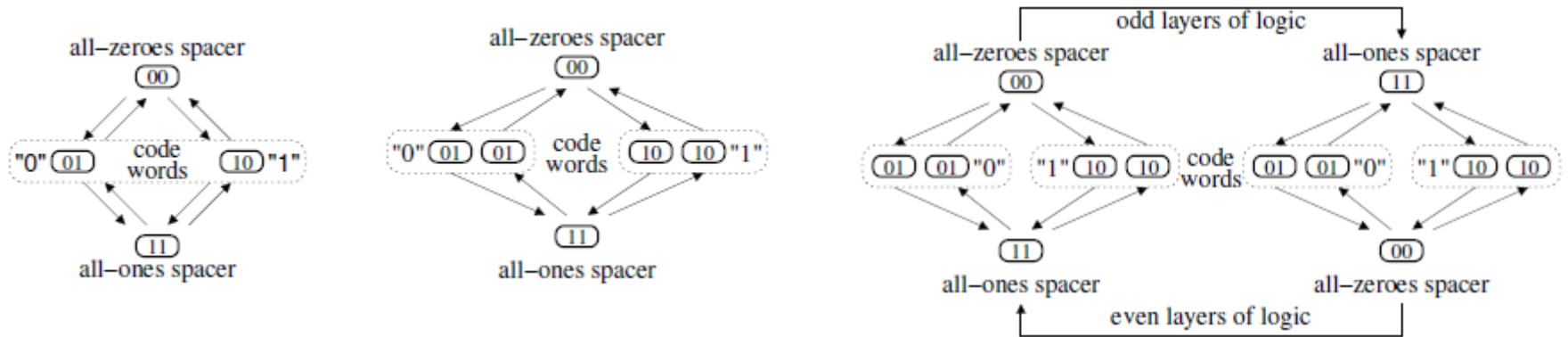


SCREEN 2:
different
(synchronous
single-rail and
power-balanced)
versions of AES S-
box.

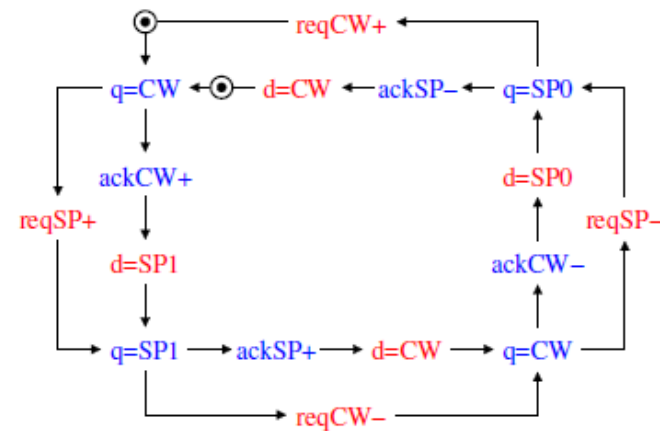
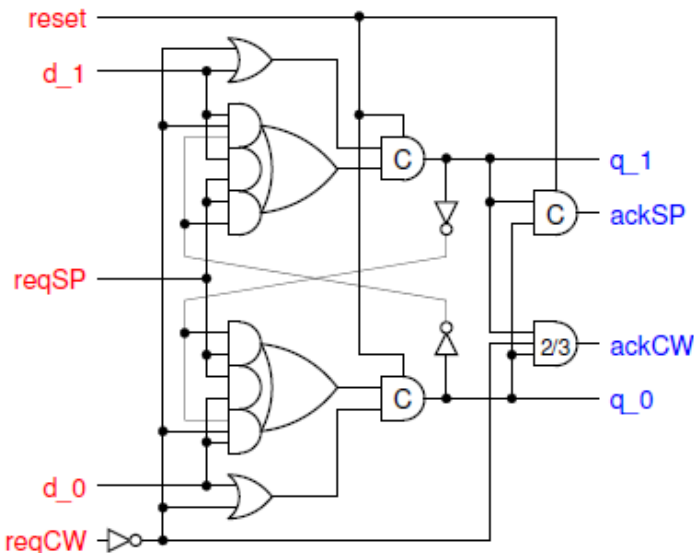


SURE:
Galois Encoded Logic AES-
128 IP core. Implements
side-channel secure "high
radix" AES-128 encryption
in a fully parallel
architecture to investigate
the security and study the
market feasibility of the
technology.

Verimap: Dual spacer and negative gate optimization

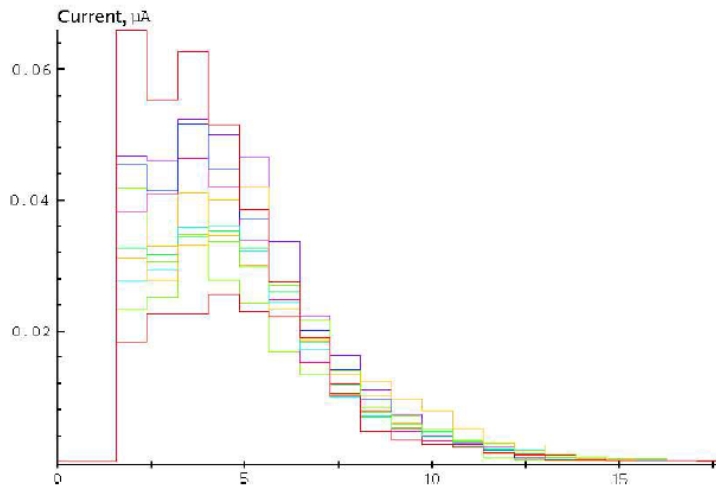


Alternating spacer dual-rail flip-flop

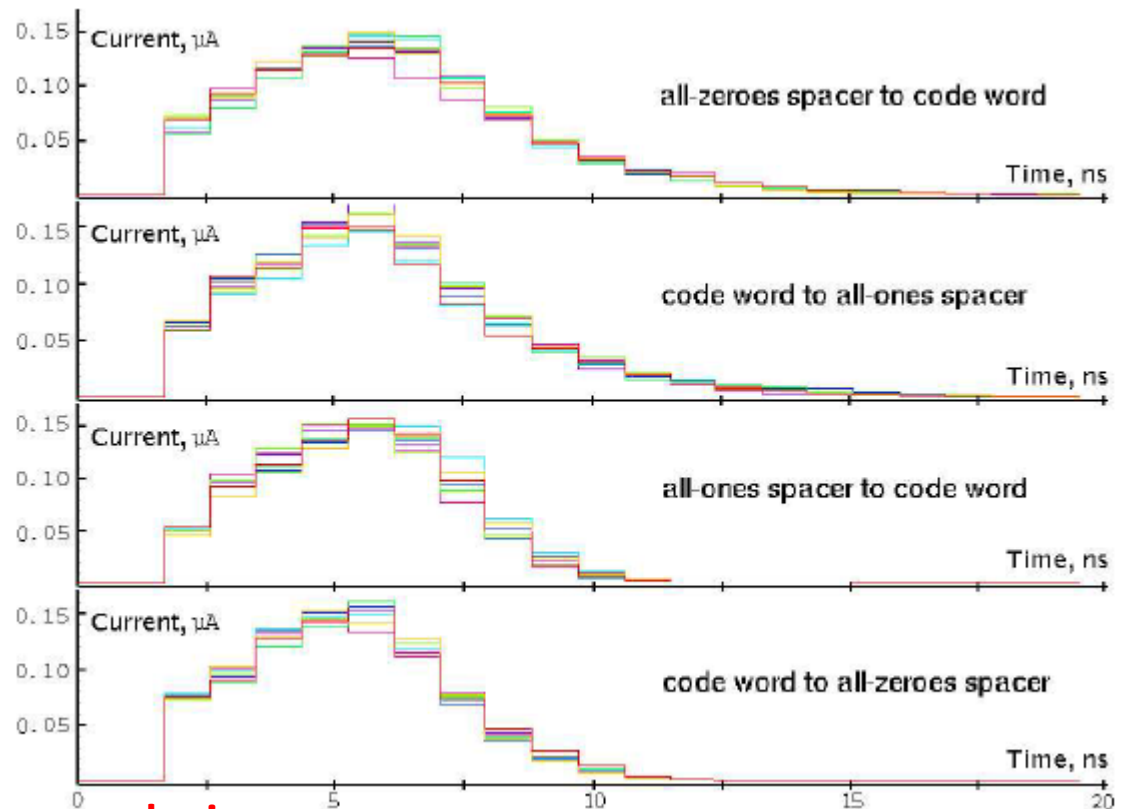


Example: Verimap AES design

Single Rail current trace



Dual Rail alternating spacer traces

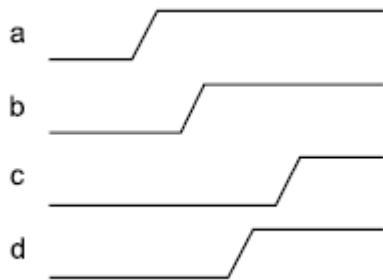


Key property of dual-rail alternating spacer logic:
For every operational cycle of the circuit all logic nodes fire => maximum power balancing

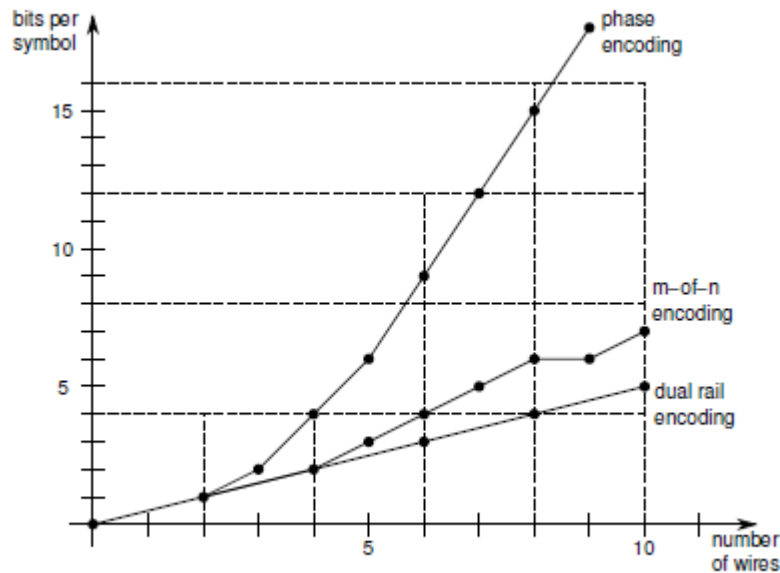
2005-2015: NoCs, FPGAs and New models

- New types of interconnects, communications, cross-talk, routing, neural network NoCs, surface wave comms, async FPGAs
- Projects: NEGUS
- People: Enzo D'Alessandro, Andrey Mokhov, Basel Halak, Sohini Dasgupta, Robin Emery, Terrence Mak, Ra'ed Aldujaili, Nizar Dahir, Ammar Karkar, Hock-Soon Low; Southampton (Bashir Al-Hashimi and Simon Ogg)
- Highlights: Phase-encoding, CPOGs, cross-talk resilient interconnects, models of GALS and wrappers, on-line deadlock detection; power/thermal model; Async FPGA flow; Chips: Negus1 and NeuralNoC

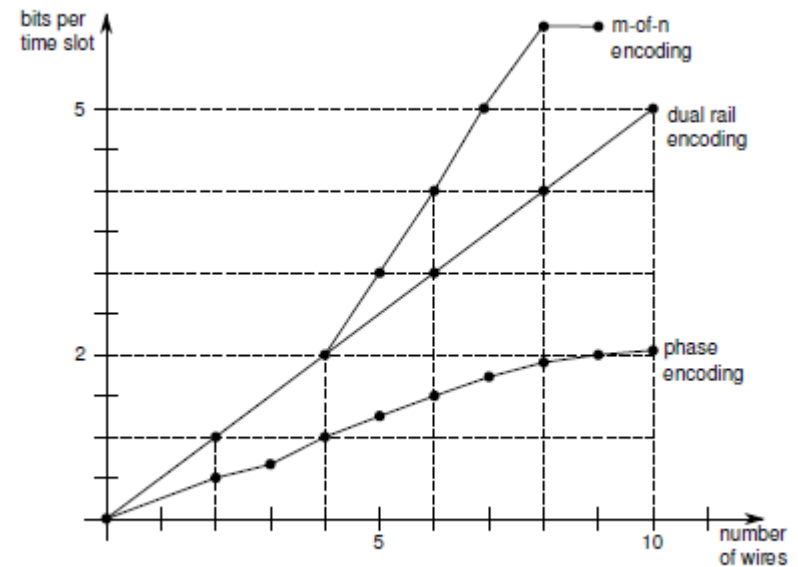
Phase encoding



An example of phase encoded symbol “*abdc*”
(total no of symbols is $4!=24$)

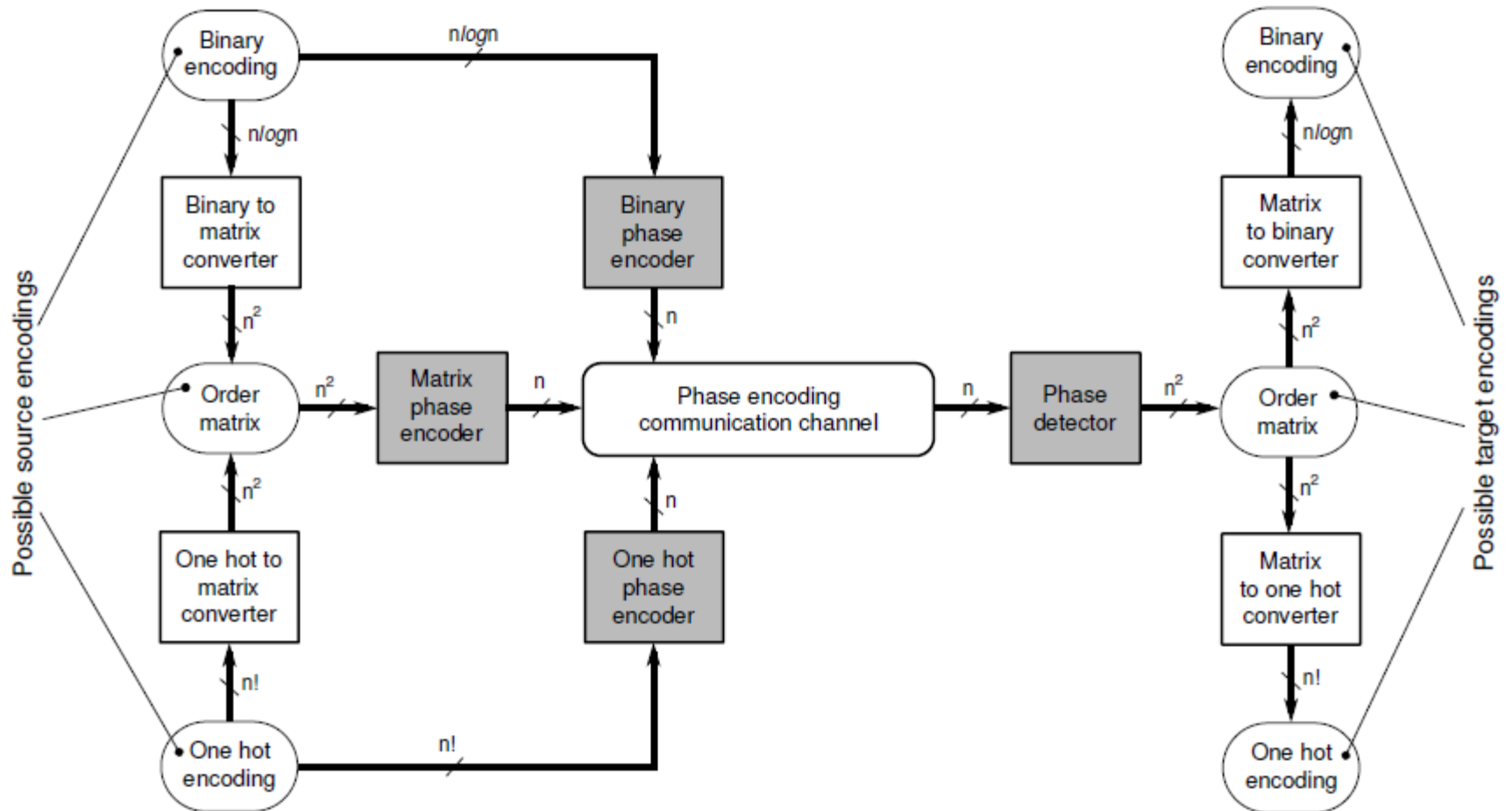


(a) number of bits per symbol

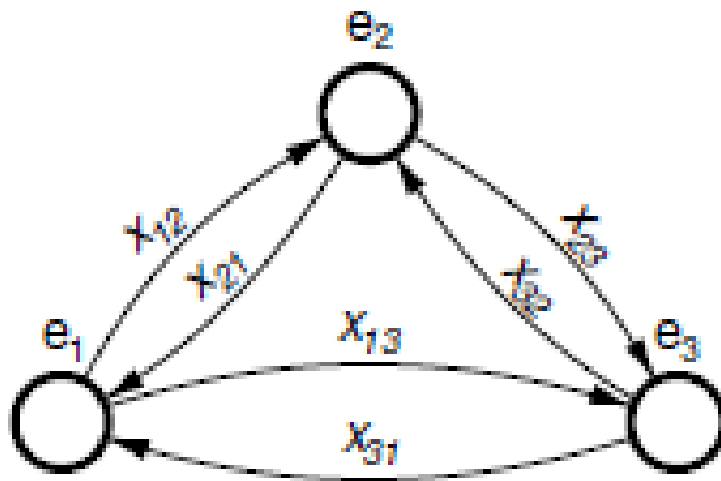


(b) number of bits per time slot

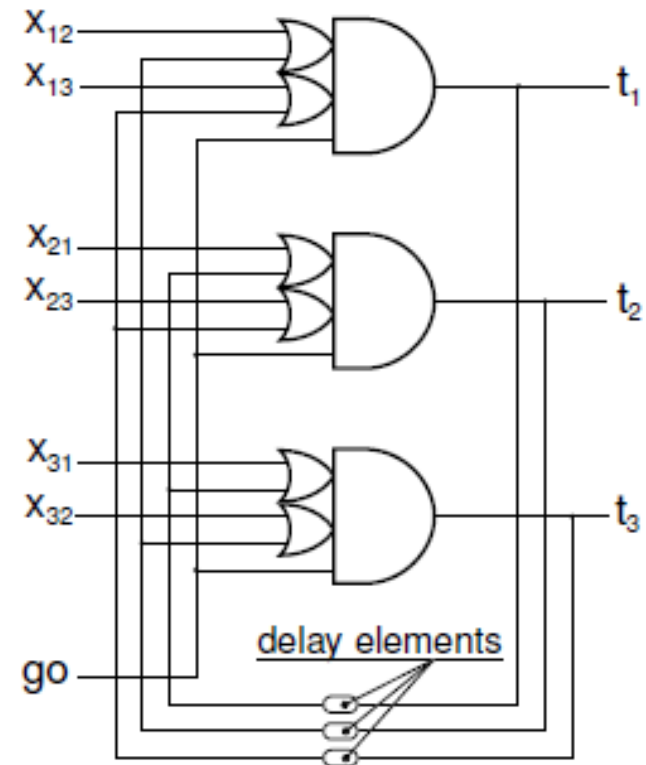
Phase encoding comms



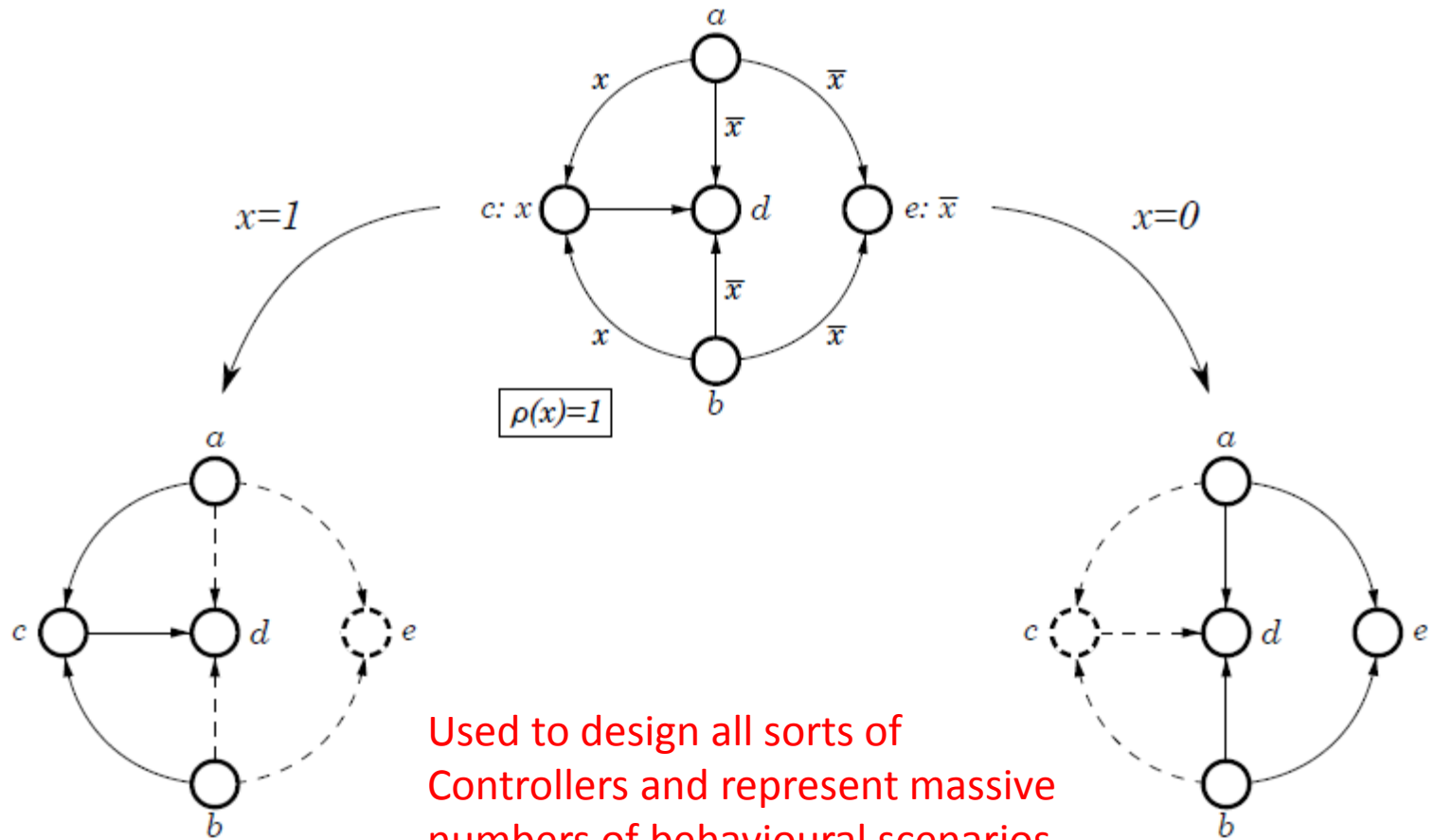
Synthesis of logic for phase encoding



(a) CPOG specification



Conditional Partial Order Graphs



Used to design all sorts of
Controllers and represent massive
numbers of behavioural scenarios
...Also led to Algebra of Graph

2005-2010: Synthesis

- Interpreted graph models, Compositionality, Data-path synthesis, SDFS and anti-tokens, Strong and Weak Indicatability, Synthesis of circuits with isochronic forks; Online data path testing
- Projects: SEDATE, VERDAD, GAEELS
- People: Ivan Poliakov, Arseniy Alekseyev, Yu Zhou (Joe), Kelvin Gardiner, Yu Li; Manchester (Doug Edwards, Will Toms, Charlie Brej), Augsburg (Walter Vogler, Dominik Wist)
- Highlights: Theory for compositions, IF relaxation; Workcraft toolkit and many plugins

Workcraft toolkit

The screenshot displays the Workcraft toolkit interface with several panels:

- dfs-all_elements - Dataflow Structure:** A hierarchical diagram showing a 'control layer' and a 'complex ST path'.
- vme_stg - Signal Transition:** A signal transition graph with nodes and edges labeled with signals like DSr+, LDS+, LDTACK+, DTACK+, DSr-, LDS-, LDTACK-, DTACK-, DSr-, LDS-, LDTACK-, DTACK-, DSr-, LDS-, LDTACK-, DTACK-.
- mayevsky_c_el2 - Digital Circuit:** A digital circuit diagram with components labeled c1, c2, c3, and c4.
- Property editor:** A panel showing 'N/A'.
- Tool controls:** A panel with playback controls (play, stop, previous, next, end) and a progress bar.
- Trace and Branch:** A table showing the current state of the system.

Trace	Branch
D-/1	
DTACK+/1	
DSw-	
DTACK-	
DSr+	DSw+
LDS-	D+/1
LDTACK-	LDS-
LDS+	LDTACK-
LDTACK+	LDS+/1
D+	LDTACK+/1
DTACK+	D-/1
- Signal and State:** A table showing the current state of the system.

Signal	State
D	0
DTACK	0
DSw	1
DSr	?
LDS	1
LDTACK	1
- Editor tools:** A panel with drawing tools (select, text, rectangle, circle, line, eraser, delete, undo, redo).
- Workspace:** A panel showing the current workspace structure.
 - Workspace
 - External
 - cpog1.work
 - dfs-all_elements.work
 - mayevsky_c_el2.work *
 - policy-test2.work
 - vme_stg.work *
 - xmas-test1.work
- Output:** A panel showing the current output of the system.


```

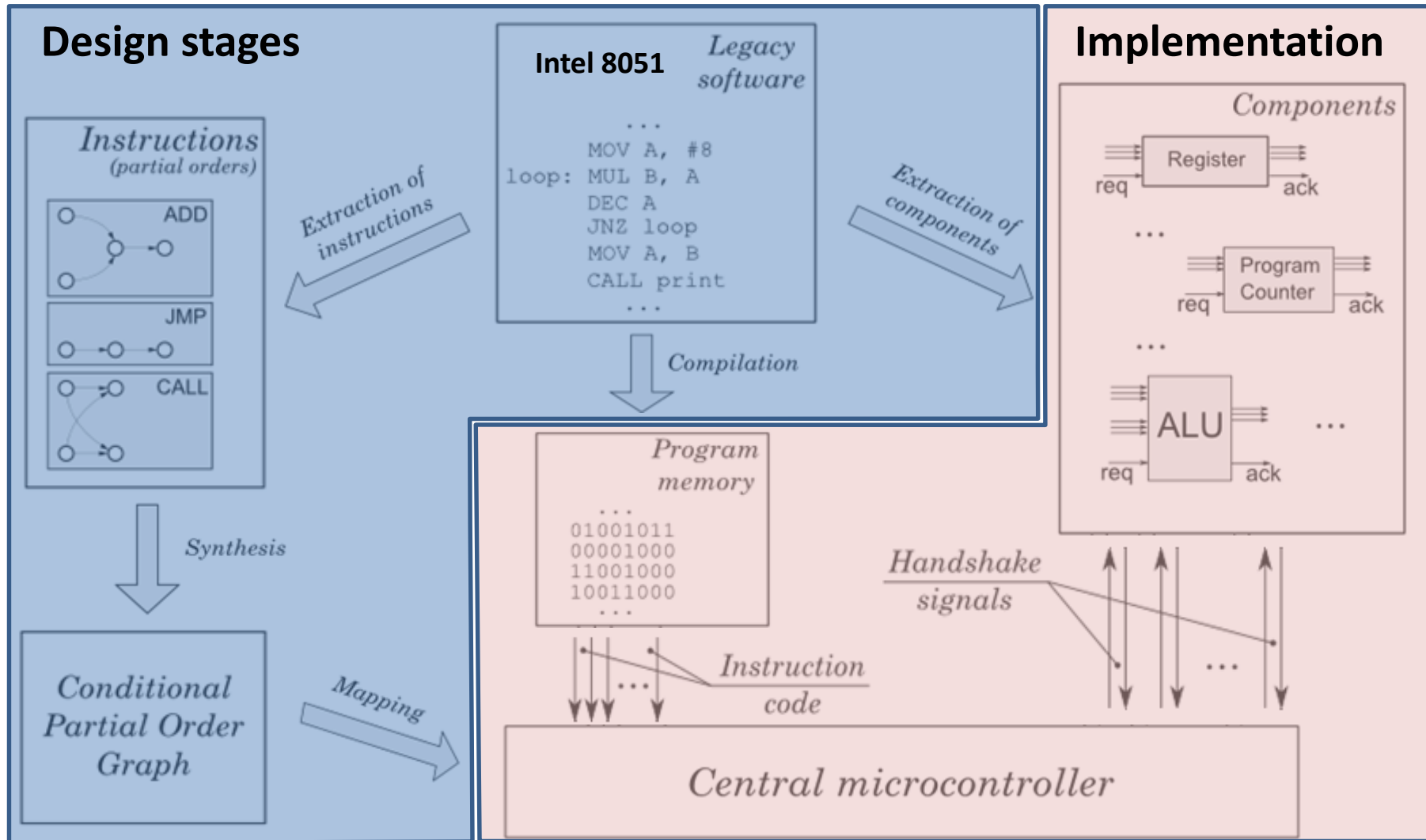
INORDER = DSr DSw LDTACK D DTACK LDS csc0;
OUTORDER = [D] [DTACK] [LDS] [csc0];
[D] = DSr LDTACK csc0' + DSw (csc0 + LDTACK');
[DTACK] = D' csc0' (DSr' + DSw) + DSw' D;
[LDS] = csc0';
[csc0] = DSr' D' (csc0 + DSw') + LDTACK csc0;

# Set/reset pins: reset(csc0)
moved from Untitled to !External/xmas-test1.work
correcting open file path...
      
```

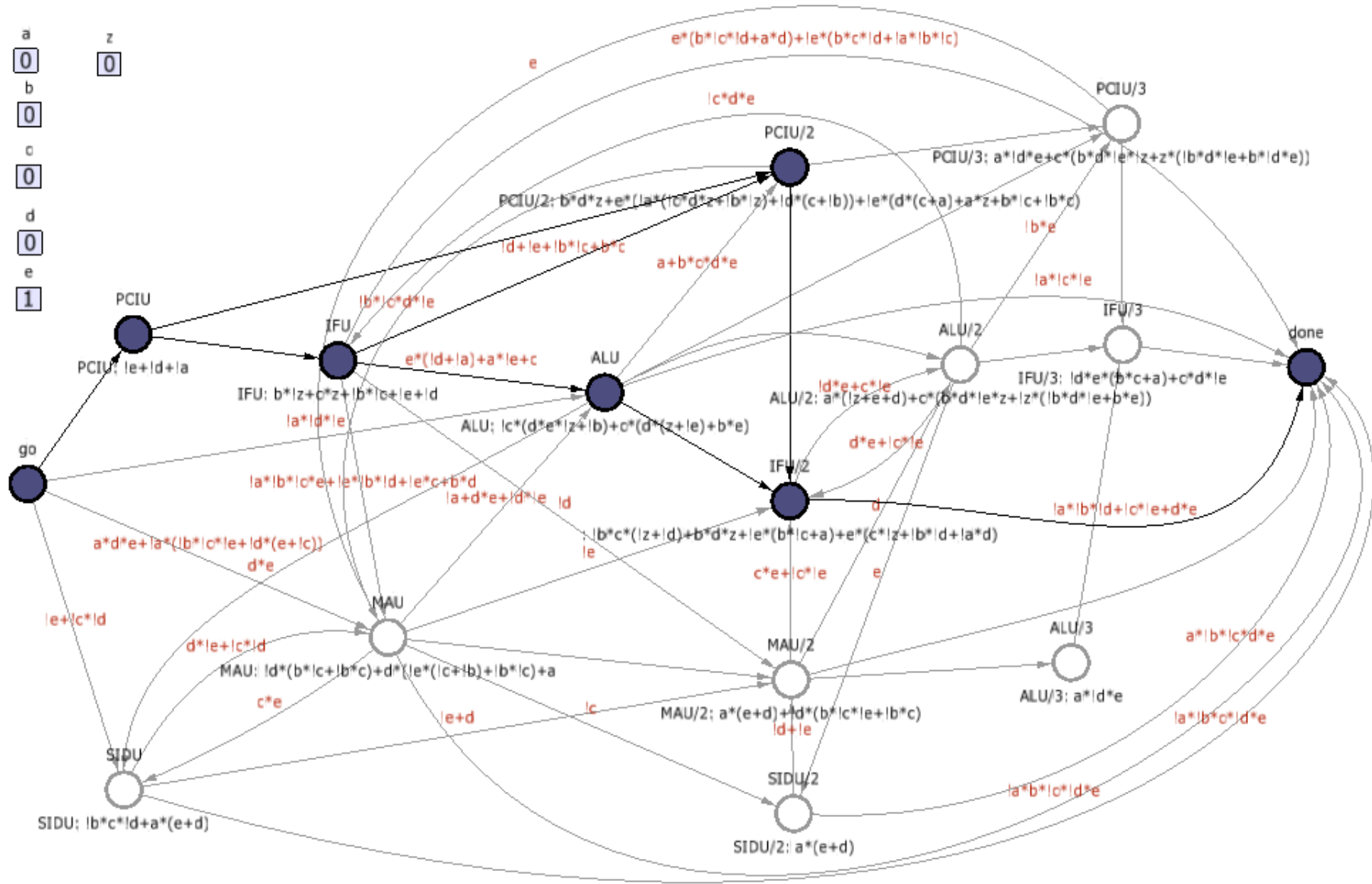

2007-2015: Low Power and Energy-modulated computing

- Low power processors, energy harvesting and async, power-proportional design, power variation resilient circuits, new power supply methods, power gating and new
- People: Chihoon Shen (Korea), Reza Ramezani, Max Rykunov, Abdullah Baz, Xuefu Zhang, Haider Alrudainy, Alessandro De Gennaro
- Highlights: low power M430, Charge-to-code converter, Speed-independent SRAM, Power-proportional 8051, CBBs versus SCCs, NEMS/MEMS for power gating; Chips: Reference-free sensor, ASRAM, 8051, Async Pipeline

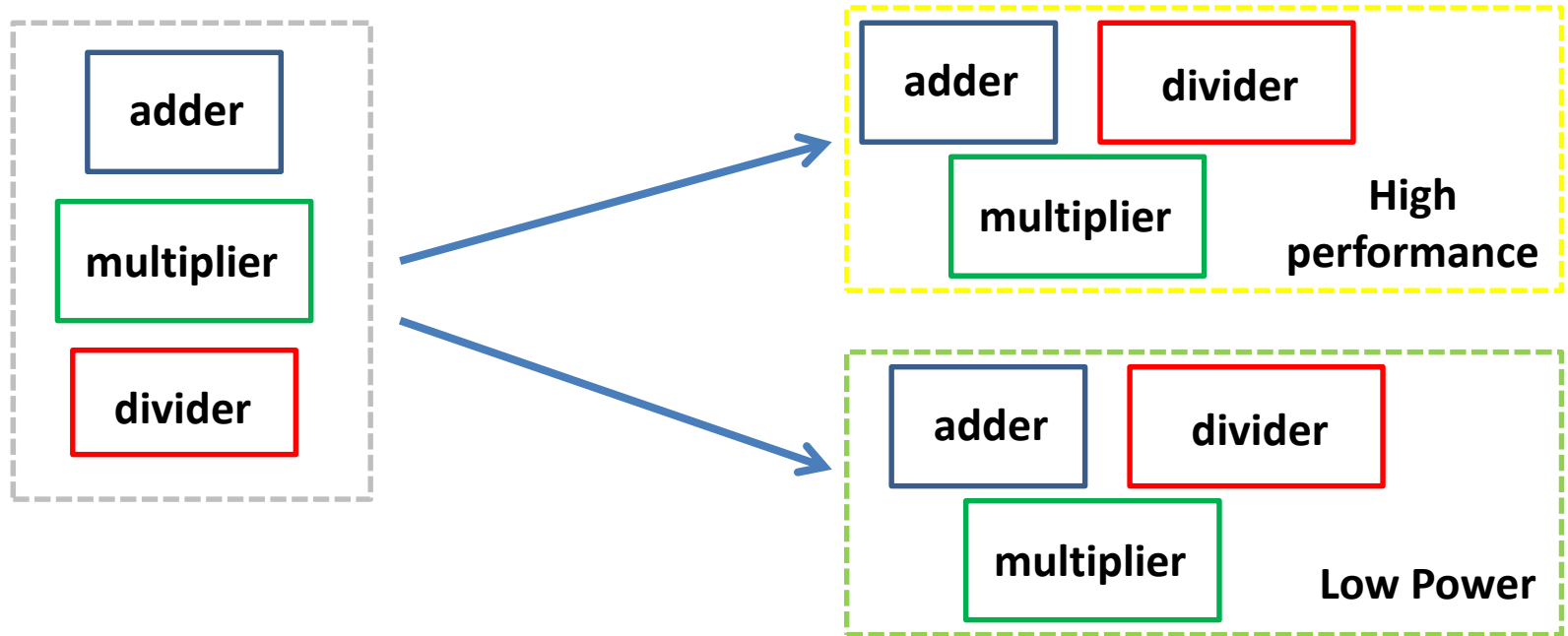
Conceptual view of the CPU design process



Intel 8051 ISA...



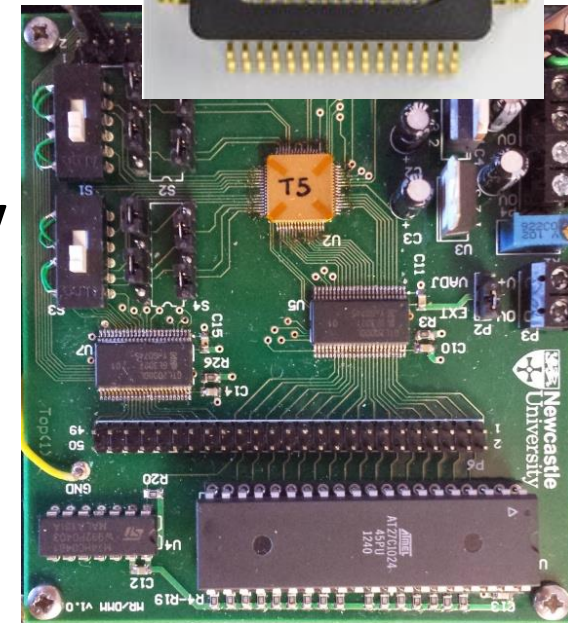
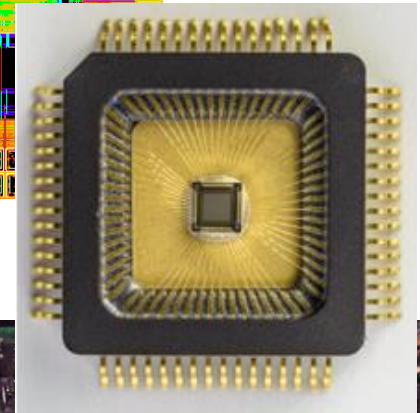
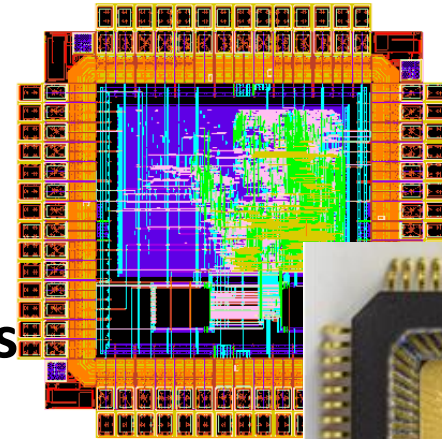
Intel 8051 Datapath...



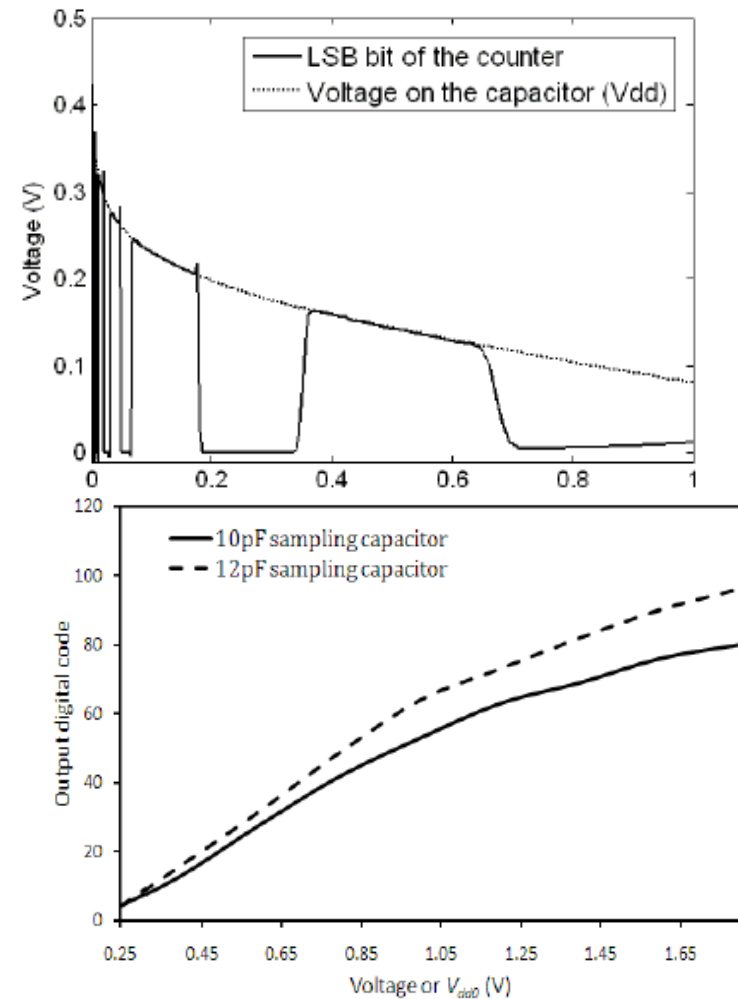
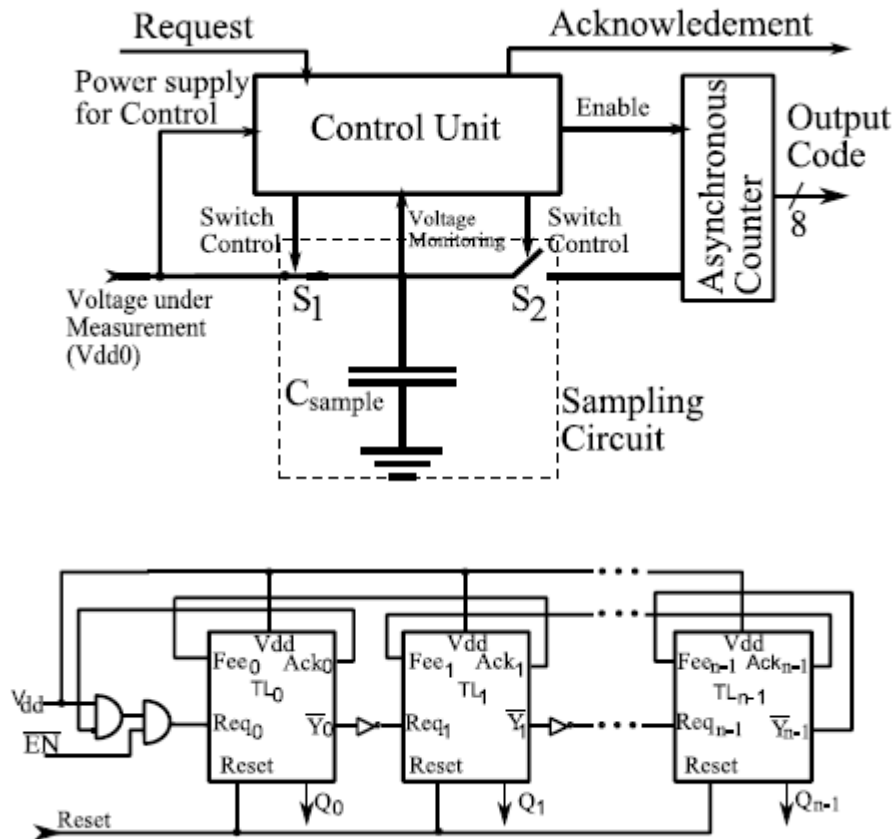
- ✓ Fully asynchronous implementation (bundled data protocol)
 - adjustable delay lines
- ✓ Fault tolerance operation
- ✓ DFT integration

Some measurements...

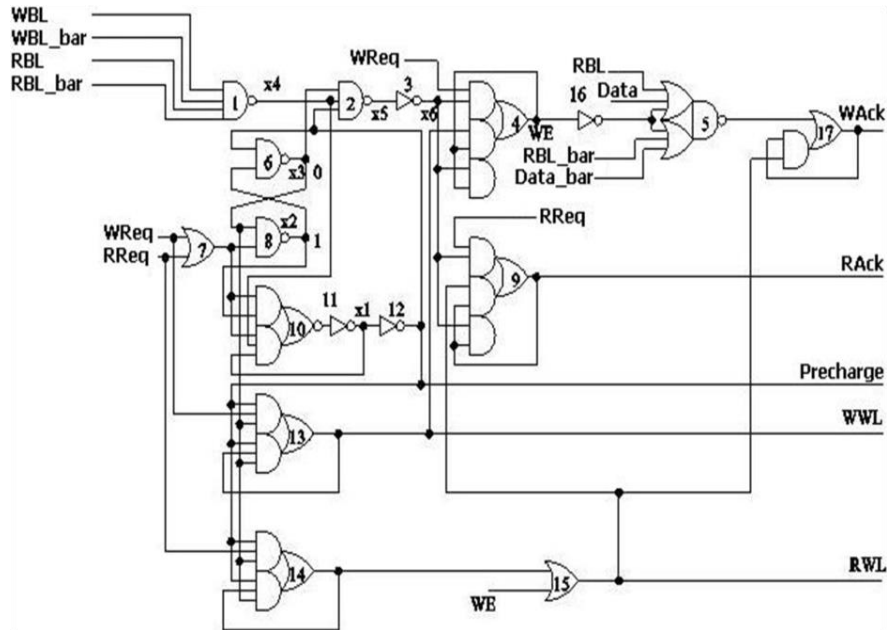
- 0.89V to 1.5V: full capability mode.
- 0.74V to 0.89V: at 0.89V the RAM starts to fail, so the chip operates using
- 0.22V to 0.74V: at 0.74V the program counter starts to fail, however the control logic synthesised using the CPOG model continues to operate correctly down to 0.22V
- 67 MIPS at 1.2 V.
- ~2700 instructions per second at 0.25V.



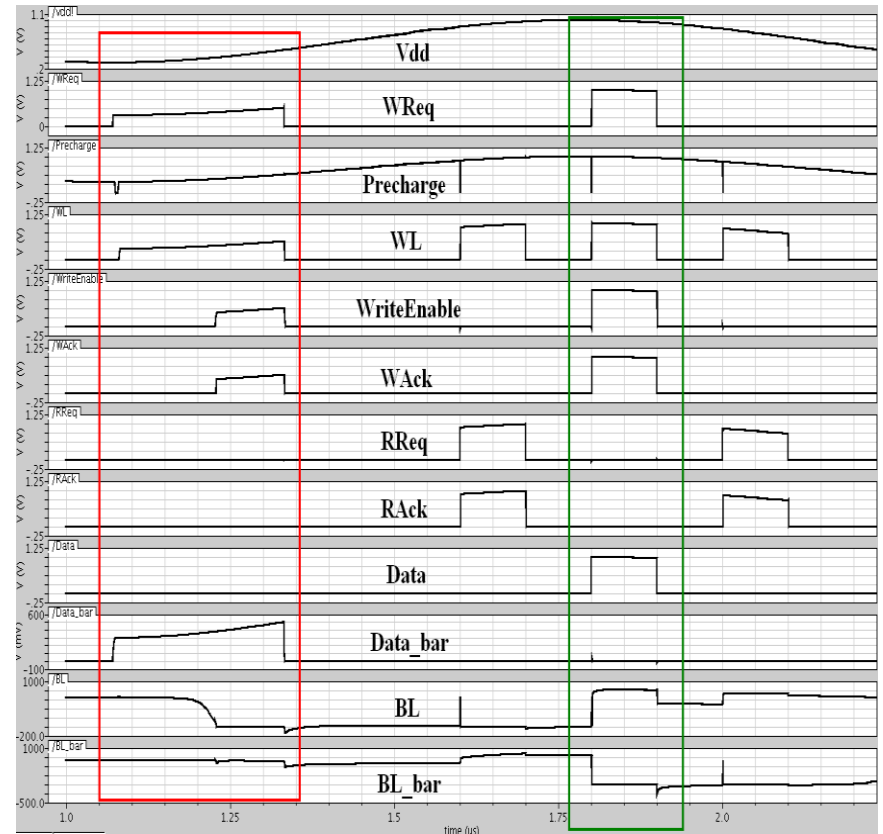
Reference-free Voltage Sensor



Self-timed SRAM



SRAM Controller



Today: living with Analog, new model mining, ...

- Asynchronous for “little digital”, self-powered sensors, ADCs; synthesis of STG specifications
- Projects: SAVVIE, A4A
- People: Kaiyuan Gao, Yuqing Xu, Vladimir Dubikhin, Jonathan Beaumont, Austin Ogwen, Benafa Oyinkuro, Sergey Mileiko; Bernard Stark (Bristol)
- Industrial collaboration: Dialog Semiconductor

Today: GALs, Many-Core, Async in Big Scale

- Globally Asynchronous Elastic Synthesis, Localities, Bundles; Event-handlers
- Project: GAELS, POETS
- People: Johnson Fernandes, Mahdi (Manchester); Southampton (Andrew Brown), ...

Thank you!