Tutorial 2 – Answers

Question 1

Let us consider first the "input" loop in the circuit for which we can write the equation below.

Equation 1: $V_{in} = V_{BE} + R_B I_B$.

There are two possibilities:

(1) The base-emitter junction is off, meaning that the transistor is in the cut-off mode.

It happens if $V_{BE} < 0.7$ volt. If it happens, then $I_B = 0$ => (equation 1) $V_{in} = V_{BE}$ => $V_{in} < 0.7$ volt.

(2) The base-emitter junction is on, meaning that the transistor is either in the forward active mode or saturation mode.

It happens if $V_{BE} \approx 0.7$ volt. If it happens, then $I_B > 0$ => (equation 1) $V_{in} > V_{BE}$ => $V_{in} > 0.7$ volt.

In this case, the base current is expressed as $I_B \approx \frac{V_{in} - 0.7}{R_B}$.

Let us now consider the "output" loop for which we can write the equations below.

Equation 2: $V_{out} = V_{CC} - R_C I_C$.

Equation 3: $V_{out} = V_{CE}$.

There are three possibilities:

(1) The transistor is in the cut-off mode (if $V_{in} < 0.7$ volt).

If it happens, then $I_B = I_C = I_E = 0$ => (equation 2) $V_{out} = V_{CC}$.

(2) The transistor is in the forward active mode (if $V_{in} > 0.7$ volt and $V_{CE} = V_{out} > V_{CE,sat}$).

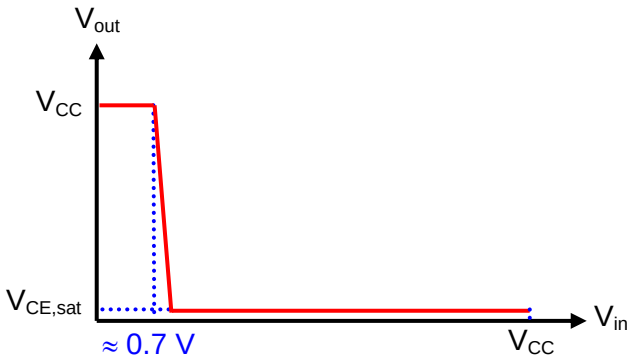
If it happens, then $I_C = \beta_F I_B$ =>

$$I_C \approx \beta_F \frac{V_{in} - 0.7}{R_B} \Rightarrow \text{(equation 2)}\ V_{out} \approx V_{CC} - \beta_F \frac{R_C}{R_B}(V_{in} - 0.7).$$

This equation remains valid as long as the condition $V_{out} > V_{CE,sat}$ is satisfied.

(3) The transistor is in the saturation mode (if $V_{in} > 0.7$ volt and $V_{CE} = V_{out} < V_{CE,sat}$).
If it happens, then $V_{out} \approx V_{CE,sat}$.

Conclusion: As V_{in} is increased beyond 0.7 volt, the transistor enters the forward active mode and the output voltage decreases according to the equation previously derived. Once V_{out} becomes equal to $V_{CE,sat}$, the transistor enters the saturation mode, and then $V_{out} \approx V_{CE,sat}$. The resulting DC transfer characteristic is shown below.



This circuit could be used as a logic inverter (see RTL, DTL, and TTL logic families, aka the saturated bipolar logic families, widely used between the 60s and the 80s).

We can also see the potential of this circuit as a voltage amplifier when the BJT is in the forward active mode. The voltage gain of this amplifier would be given by

$$A_v = -\beta_F \frac{R_C}{R_B}.$$

Question 2

In Question 1 of Tutorial 2, we showed that, as long as the BJT operates in the forward active mode of operation, the output voltage $V_{out}(t)$ is given by

$$V_{out}(t) \approx V_{CC} - R_C \beta_F \frac{V_{in}(t) - 0.7}{R_B}.$$

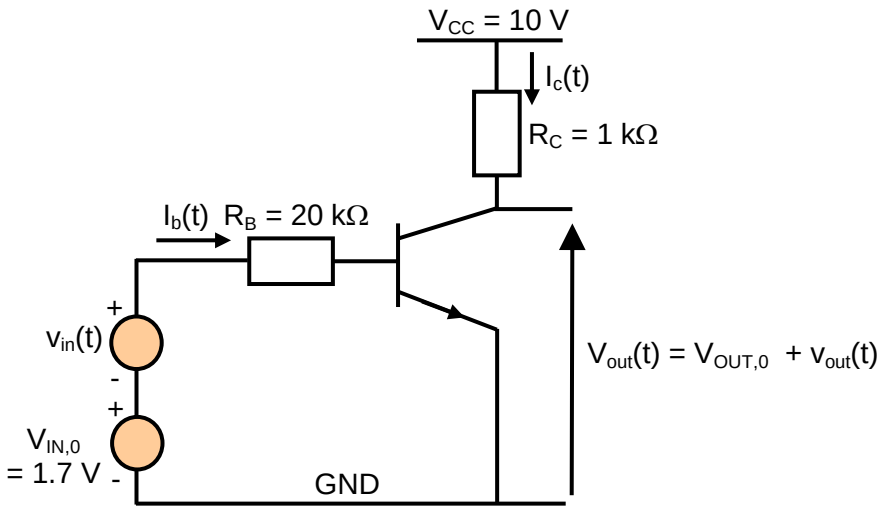
Assume that $V_{in}(t) = V_{IN,0} + v_{in}(t)$, where $V_{IN,0}$ denotes a DC voltage and $v_{in}(t)$ designates the AC signal to be amplified. In this case, we can write:

$$V_{out}(t) \approx V_{CC} - \beta_F \frac{R_C}{R_B}(V_{IN,0} - 0.7) - \beta_F \frac{R_C}{R_B} v_{in}(t) = V_{OUT,0} + v_{out}(t),$$

where $V_{OUT,0}$ denotes a DC voltage and $v_{out}(t)$ is the amplified replica of the input AC signal. Since the voltage gain must be equal to -5, we must have

$$A_V = \frac{v_{out}(t)}{v_{in}(t)} = -\beta_F \frac{R_C}{R_B} = -5.$$

Here, we choose R_C = 1 kΩ and R_B = 20 kΩ, for instance.



The DC voltages $V_{IN,0}$ and $V_{OUT,0}$ are the *bias voltages*. Their values can be chosen by the circuit designer so that the amplifier operates right in the middle of the forward active region. In fact, in

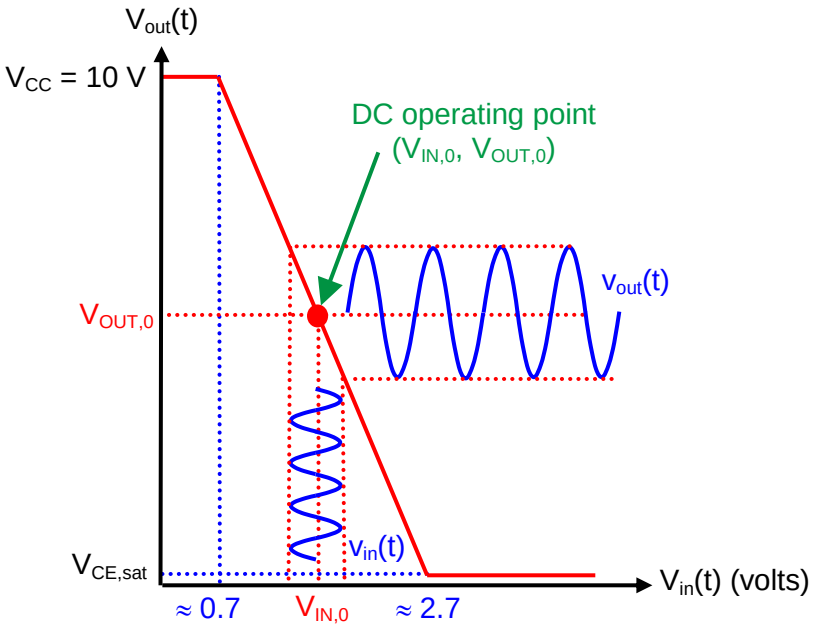
order to maximise the maximum output voltage swing, our goal is to have $V_{OUT,0}$ midway between V_{CC} and $V_{CE,sat}$:

$$V_{OUT,0} = \frac{V_{CC} + V_{CE,sat}}{2} \approx 5.1 \text{ volts},$$

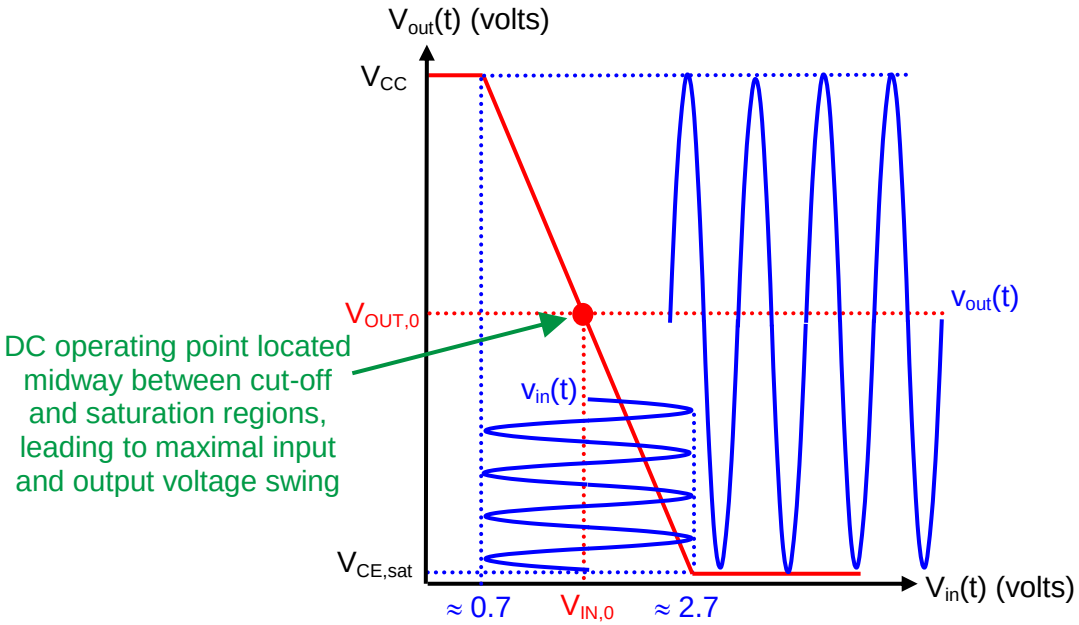
which leads to $V_{IN,0} = 0.7 + \frac{R_B}{2\beta_F R_C} V_{CC} \approx 1.7$ volts.

Note that this circuit is able to amplify and track changes in $v_{in}(t)$ as long as the BJT remains within the limits set by cut-off and saturation. If the magnitude of $v_{in}(t)$ increases beyond those limits, the output voltage $v_{out}(t)$ is clipped and distortion then occurs.

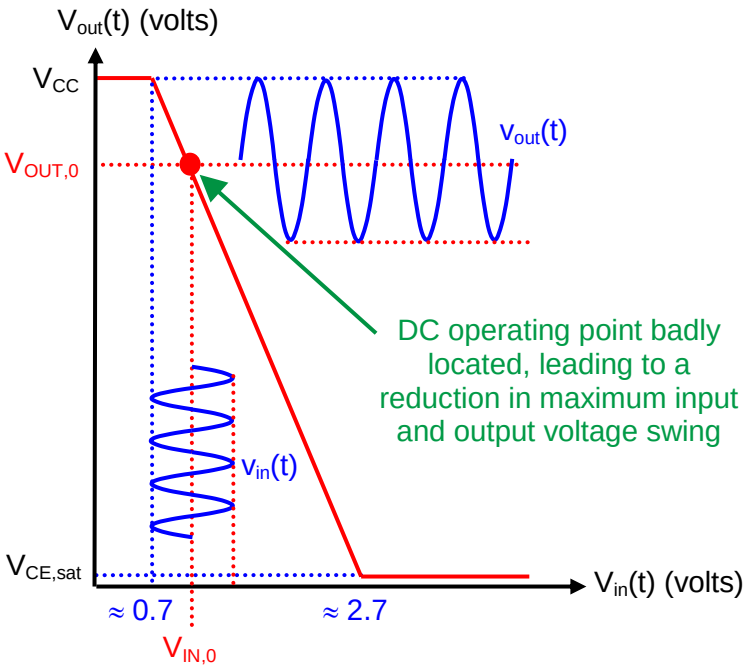
Note that we employ two power supplies to bias the BJT. With a smarter biasing technique, a single power supply is in fact sufficient.



• An ideally located DC operating point (optimal biasing) allows maximal swings for both input and output voltages, as illustrated below.



• A badly located DC operating point (non-optimal biasing) can significantly reduce the maximal swings for both input and output voltages, as illustrated below.



• If the transistor is allowed to enter either the cut-off mode or the saturation mode, the output signal is clipped, and distortion is thus introduced. Our circuit is no longer a linear amplifier.