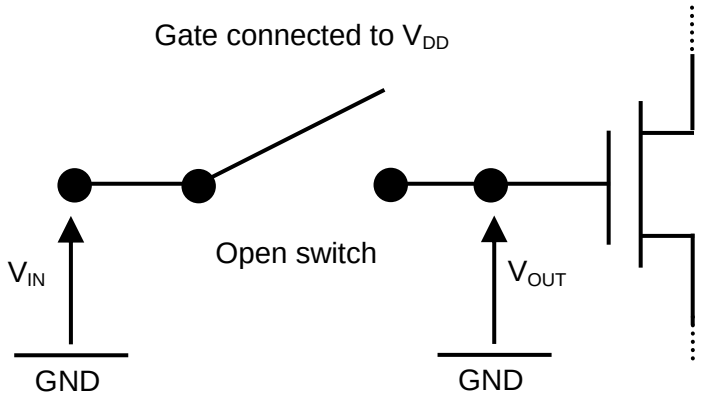
Tutorial 5 – Answers

Question 1

(1) The gate is connected to V_{DD}.

In this case, we can write $V_{GS} = V_{DD} – V_{OUT}$ and $V_{DS} = V_{IN} – V_{OUT}$.

Since all voltage values in the circuit range from 0 to V_{DD}, $V_{DD} – V_{OUT}$ is always positive and thus higher than the threshold voltage V_{TP} (< 0 for a PMOS transistor). This means that $V_{GS} > V_{TP}$. The PMOS transistor is in the cut-off mode of operation and thus equivalent to an open switch since the drain is not connected to the source.



(2) The gate is connected to ground.

In this case, we can write $V_{GS} = – V_{OUT}$ and $V_{DS} = V_{IN} – V_{OUT}$.

The transistor is in the cut-off mode when $V_{GS} > V_{TP}$, i.e. $– V_{OUT} > V_{TP}$ => $V_{OUT} < |V_{TP}|$. In this case, the transistor is equivalent to an open switch since the drain is not connected to the source.

The transistor is in the linear mode when $V_{GS} \le V_{TP}$, i.e. $V_{OUT} \ge |V_{TP}|$, and $V_{DS} > V_{GS} - V_{TP}$, i.e. $V_{IN} - V_{OUT} > -V_{OUT} - V_{TP}$, i.e. $V_{IN} > |V_{TP}|$. In this case, the drain current I_D is given by

$$I_D = k_p\left(-V_{OUT} - V_{TP} - \frac{V_{IN} - V_{OUT}}{2}\right)(V_{IN} - V_{OUT}) = 0.$$

$$\Rightarrow \quad \left(|V_{TP}| - \frac{V_{IN}}{2} - \frac{V_{OUT}}{2}\right)(V_{IN} - V_{OUT}) = 0.$$

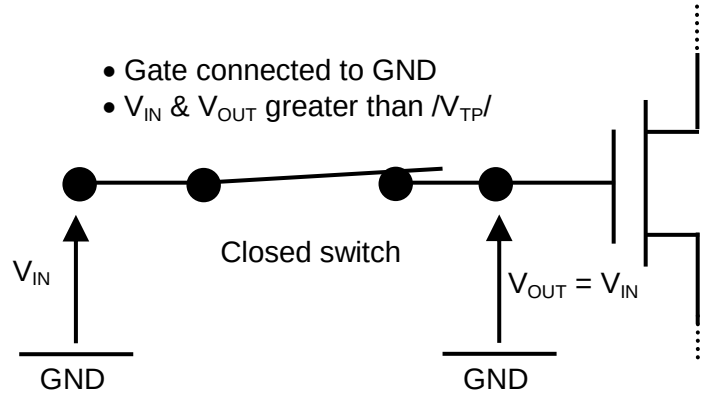
There are two possible solutions to this equation:

(a) $|V_{TP}| - \frac{V_{IN}}{2} - \frac{V_{OUT}}{2} = 0$ => $V_{OUT} = 2|V_{TP}| - V_{IN}$.

(b) $V_{IN} - V_{OUT} = 0$ => $V_{OUT} = V_{IN}$.

The solution (a) must be discarded as it is incompatible with the conditions necessary for the transistor to be in the linear mode. On the other hand, the solution (b) is compatible with those conditions.

Our conclusion is that, when $V_{OUT} \ge |V_{TP}|$ and $V_{IN} > |V_{TP}|$, we have $V_{OUT} = V_{IN}$ and the transistor is thus equivalent to a closed switch.



Note that this closed switch exhibits a resistance R given by

$$R = -\frac{dV_{DS}}{dI_D}\bigg|_{V_{DS}=V_{IN}-V_{OUT},\,V_{GS}=-V_{OUT}} = -\frac{1}{k_p\left(-V_{OUT}-V_{TP}-V_{IN}+V_{OUT}\right)} = \frac{1}{k_p\left(V_{IN}-|V_{TP}|\right)}$$

.

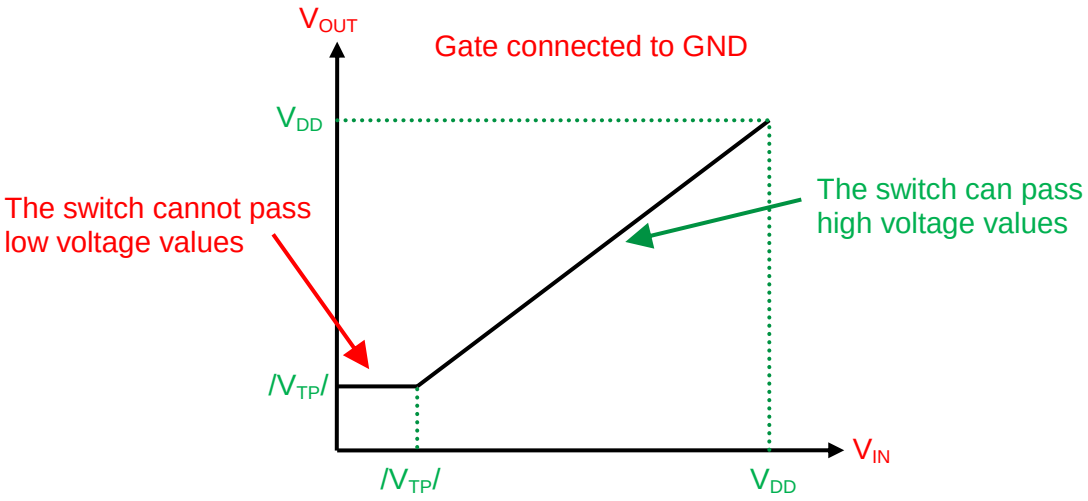
There is no voltage drop across this resistance because the current flowing through the switch is equal to zero. Therefore, the presence of this resistance R is not an issue, as long as R does not become infinite...

The transistor is in the saturation mode when $V_{GS} \le V_{TP}$, i.e. $V_{OUT} \ge |V_{TP}|$, and $V_{DS} \le V_{GS} - V_{TP}$, i.e. $V_{IN} - V_{OUT} \le -V_{OUT} - V_{TP}$ => $V_{IN} \le |V_{TP}|$. In this case, the drain current I_D is given by

$$I_D = \frac{k_p}{2}\left(V_{GS}-V_{TP}\right)^2 = 0$$

$$\Rightarrow \quad I_D = \frac{k_p}{2}\left(-V_{OUT}+|V_{TP}|\right)^2 = 0 \;\Rightarrow\; V_{OUT} = |V_{TP}|.$$

We thus conclude that, when $V_{OUT} \ge |V_{TP}|$ and $V_{IN} \le |V_{TP}|$, we have $V_{OUT} = |V_{TP}|$ and the switch output is then constant.

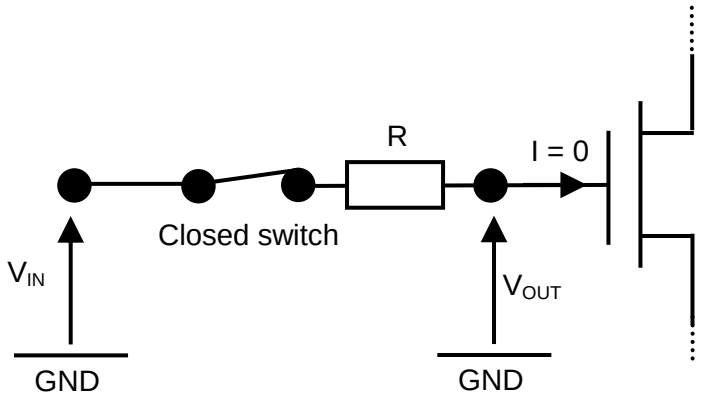


As a summary, a PMOS transistor can be thought of as a switch controlled by its gate voltage. The switch is closed when the voltage applied on the gate is low (e.g., equal to ground), and is

open when this gate voltage is high (e.g., equal to V_{DD}). However, this switch is imperfect because, when closed, it cannot pass voltage values that are below $|V_{TP}|$.

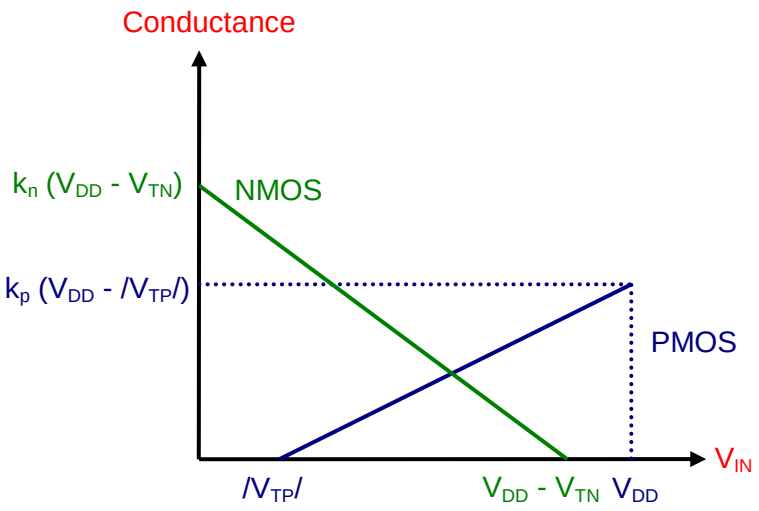
Question 2

When the switch is closed, we need to make sure that the resistance associated with it never becomes infinite. To understand this point, we can consider the circuit depicted below.

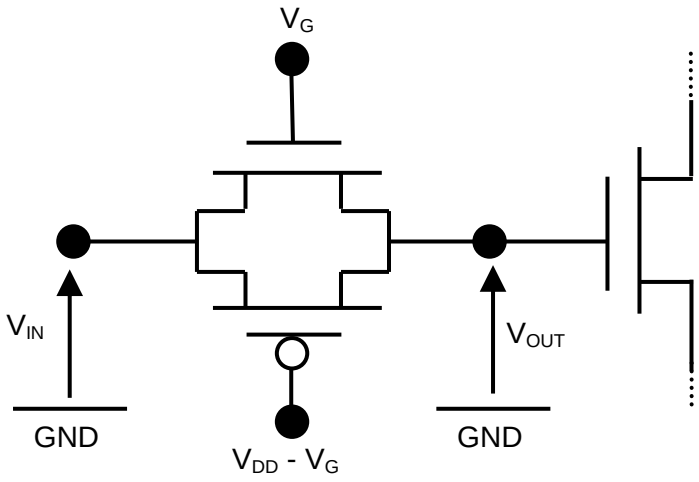


It appears that $V_{IN} - V_{OUT} = RI$. Since I = 0, we have $V_{OUT} = V_{IN}$ as long as R is not infinite. If we think in terms of conductance instead of resistance, we can state that $V_{OUT} = V_{IN}$ as long as the conductance G = 1/R associated with the closed switch is not equal to zero.

The conductance of an NMOS transistor used as a closed switch is given by $G_N = k_n (V_{DD} - V_{TN} - V_{IN})$, whereas the conductance of a PMOS transistor used as a closed switch is given by $G_P = k_p (V_{IN} - |V_{TP}|)$.



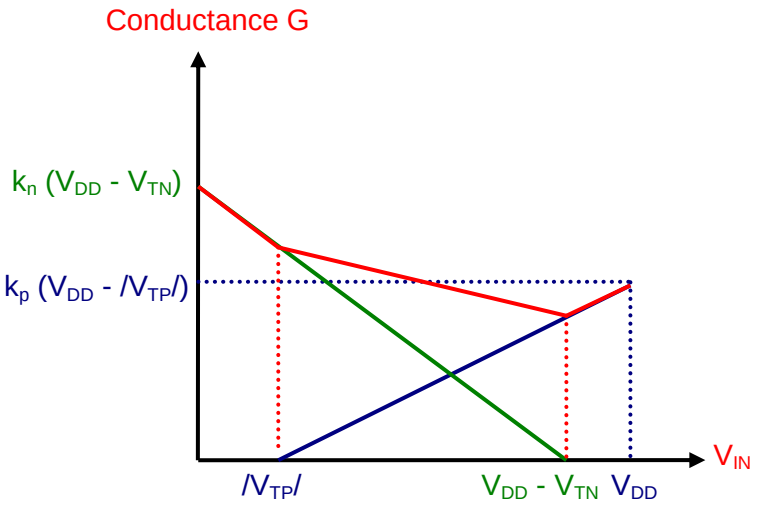
To design a switch whose conductance never becomes equal to zero, we can simply connect an NMOS transistor in parallel with a PMOS transistor as shown below.



If the voltage V_G applied on the gate of the NMOS is equal to 0 V, the voltage applied on the gate of the PMOS transistor is then equal to $V_{DD} - V_G = V_{DD}$. In this case, both transistors are in the cut-off mode of operation, and the whole structure is equivalent to an open switch.

If the voltage V_G applied on the gate of the NMOS is equal to V_{DD}, the voltage applied on the gate of the PMOS transistor is then equal to $V_{DD} – V_{DD} = 0$. In this case, both transistors are equivalent to imperfect switches.

Since both transistors are connected in parallel, the conductance G of the whole structure is expressed as $G = G_N + G_P$. Since G is never equal to zero (and even relatively constant), this circuit is then equivalent to a perfect closed switch that can pass all voltage values ranging from 0 to V_{DD}.



Question 3

(a) Logic Inverter: $V_{OUT} = \overline{V}_{IN}$, (b) NOR logic gate: $V_{OUT} = \overline{V_1 + V_2}$, (c) NAND logic gate: $V_{OUT} = \overline{V_1 \cdot V_2}$, (d) Multiplexer: $V_{OUT} = V_1 \cdot V_3 + V_2 \cdot \overline{V}_3$, (d) XNOR logic gate: $V_{OUT} = V_1 \cdot V_2 + \overline{V}_1 \cdot \overline{V}_2$.

In all cases, the current drawn from the power supply is equal to zero since the output of each circuit is connected to the gates of MOSFETs. This is a very important result as it implies that the power consumption of these five CMOS circuits is equal to zero when the input voltages are equal to either 0 or V_{DD}. Therefore, a very high density of integration can be achieved with CMOS digital circuits.