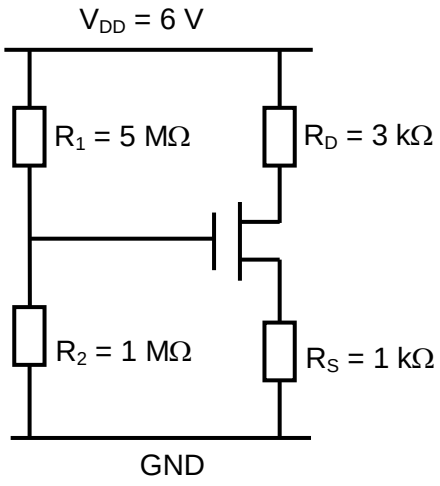
Tutorial 6 – Answers

Question 1

For the DC analysis, we need to consider the circuit depicted below. We assume that the NMOS transistor is in the saturation mode (to be checked later).



Due to the voltage divider formed by R_1 and R_2, we can show that the gate voltage V_G (with respect to ground) is given by $V_G = \frac{R_2}{R_1 + R_2} V_{DD}$ = 1 V. Then, we can write $V_G = V_{GS0} + R_S I_{D0}$.

Since we also have $I_{D0} = \frac{k_n}{2}(V_{GS0} - V_{TN})^2$, the voltage V_{GS0} is computed by solving the following quadratic equation: $V_G = V_{GS0} + \frac{R_S k_n}{2}(V_{GS0} - V_{TN})^2$, which can be written as

$$\frac{R_S k_n}{2}(V_{GS0})^2 + (1 - R_S k_n V_{TN}) V_{GS0} + \left(\frac{R_S k_n}{2} V_{TN}^2 - V_G\right) = 0 .$$

Solving this equation leads to

$$V_{GS0} = \frac{R_S k_n V_{TN} - 1 + \sqrt{1 + 2R_S k_n (V_G - V_{TN})}}{R_S k_n} = 0.75 \text{ V},$$

$$V_{GS0} - V_{TN} = \frac{-1 + \sqrt{1 + 2R_S k_n (V_G - V_{TN})}}{R_S k_n} = 0.25 \text{ V},$$

$$\text{and } I_{D0} = \frac{1 + R_S k_n (V_G - V_{TN}) - \sqrt{1 + 2R_S k_n (V_G - V_{TN})}}{R_S^2 k_n} = 250 \ \mu\text{A}.$$

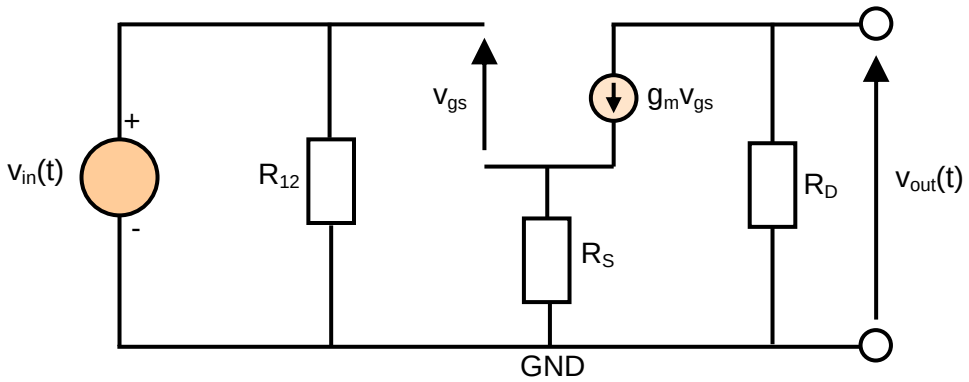
Since $V_{GS0} > V_{TN}$, the NMOS transistor is either in the linear mode or the saturation mode.

Finally, we can compute the value of the DC voltage V_{DS0} as $V_{DS0} = V_{DD} - (R_D + R_S) I_{D0}$ = 5 V. Since $V_{DS0} > V_{GS0} - V_{TN}$, we conclude that our assumption was right and the NMOS transistor is indeed in the saturation mode.

The DC analysis also allows us to determine the transconductance of the NMOS transistor:

$$g_m = k_n (V_{GS0} - V_{TN}) = \frac{-1 + \sqrt{1 + 2R_S k_n (V_G - V_{TN})}}{R_S} = 2 \text{ mS}.$$

As for the AC analysis, the small-signal model of our common-source amplifier with negative feedback is depicted below.



The resistance R_{12} is given by $R_{12} = \frac{R_1 R_2}{R_1 + R_2} \approx 833 \text{ k}\Omega$.

We can show that $v_{out}(t) = -R_D\, g_m\, v_{gs}$.

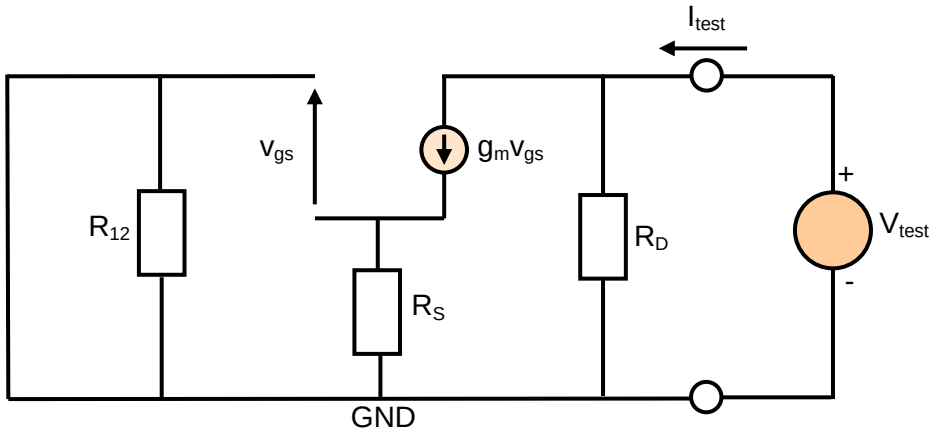
In addition, we can write $v_{in}(t) = v_{gs} + R_S\, g_m\, v_{gs} = (1 + R_S\, g_m)\, v_{gs}$.

The small-signal voltage gain of the common-source amplifier with negative feedback is thus given by

$$A_v = \frac{v_{out}(t)}{v_{in}(t)} = -\frac{R_D\, g_m}{1 + R_S\, g_m} = -2.$$

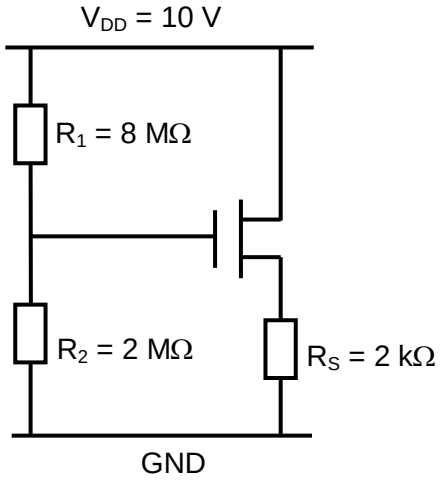
The small-signal input resistance is given by $r_{in} = R_{12} \approx 833\ \text{k}\Omega$. This is a very large value.

The small-signal output resistance is given by $r_{out} = R_D = 3\ \text{k}\Omega$. This result comes from the fact that, in the circuit depicted below, $v_{gs} = -R_S\, g_m\, v_{gs}$, which is possible only if $v_{gs} = 0$.



Question 2

For the DC analysis, we need to consider the circuit depicted below. We assume that the NMOS transistor is in the saturation mode (to be checked later).



Due to the voltage divider formed by R_1 and R_2, we can show that the gate voltage V_G (with respect to ground) is given by $V_G = \frac{R_2}{R_1 + R_2} V_{DD}$ = 2 V. Then, we can write $V_G = V_{GS0} + R_S I_{D0}$.

Since we also have $I_{D0} = \frac{k_n}{2}(V_{GS0} - V_{TN})^2$, the voltage V_{GS0} is computed by solving the following quadratic equation: $V_G = V_{GS0} + \frac{R_S k_n}{2}(V_{GS0} - V_{TN})^2$, which can be written as

$$\frac{R_S k_n}{2}(V_{GS0})^2 + (1 - R_S k_n V_{TN}) V_{GS0} + \left(\frac{R_S k_n}{2} V_{TN}{}^2 - V_G\right) = 0 .$$

Solving this equation leads to

$$V_{GS0} = \frac{R_S k_n V_{TN} - 1 + \sqrt{1 + 2R_S k_n (V_G - V_{TN})}}{R_S k_n} \approx 1.30 \text{ V},$$

$$V_{GS0} - V_{TN} = \frac{-1 + \sqrt{1 + 2R_S k_n (V_G - V_{TN})}}{R_S k_n} \approx 0.30 \text{ V},$$

$$\text{and } I_{D0} = \frac{1 + R_S k_n (V_G - V_{TN}) - \sqrt{1 + 2R_S k_n (V_G - V_{TN})}}{R_S{}^2 k_n} \approx 352 \ \mu\text{A}.$$

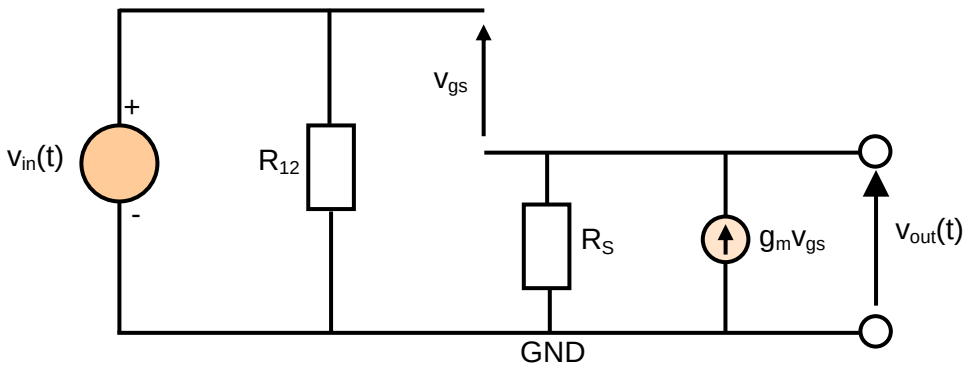
Since $V_{GS0} > V_{TN}$, the NMOS transistor is either in the linear mode or the saturation mode.

Finally, we can compute the value of the DC voltage V_{DS0} as $V_{DS0} = V_{DD} - R_S I_{D0} \approx 9.3$ V. Since $V_{DS0} > V_{GS0} - V_{TN}$, we conclude that our assumption was right and the NMOS transistor is indeed in the saturation mode.

The DC analysis also allows us to determine the transconductance of the NMOS transistor:

$$g_m = k_n (V_{GS0} - V_{TN}) = \frac{-1 + \sqrt{1 + 2R_S k_n (V_G - V_{TN})}}{R_S} \approx 2.4 \text{ mS}.$$

As for the AC analysis, the small-signal model of our common-drain amplifier is depicted below.



The resistance R_{12} is given by $R_{12} = \frac{R_1 R_2}{R_1 + R_2}$ = 1.6 MΩ.

We can show that $v_{out}(t) = g_m R_S v_{gs}$.

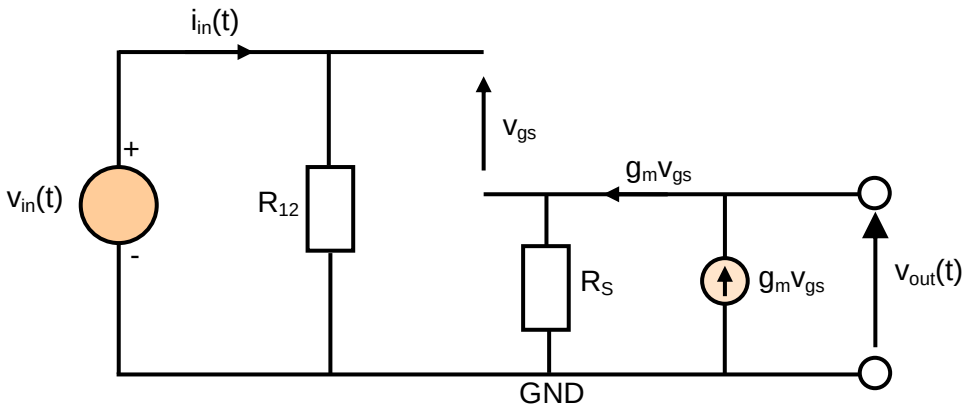
In addition, we can write: $v_{in}(t) = v_{gs} + g_m R_S v_{gs} = (1 + g_m R_S) v_{gs}$.

The small-signal voltage gain of the common-drain amplifier is thus given by

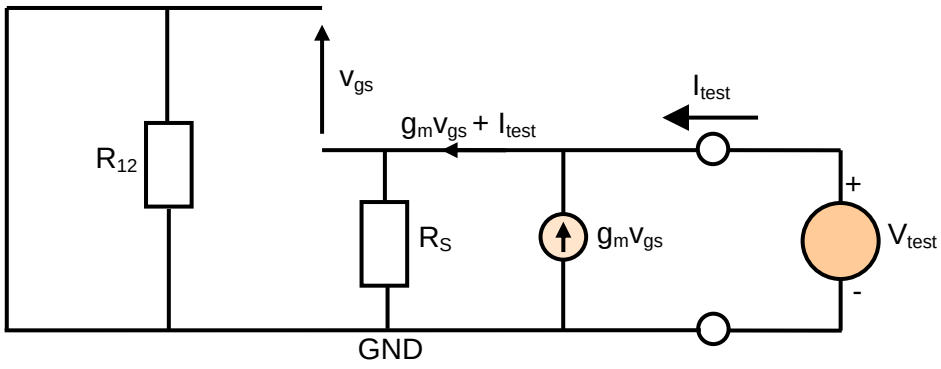
$$A_v = \frac{v_{out}(t)}{v_{in}(t)} = \frac{g_m R_S}{1 + g_m R_S} \approx 0.83.$$

The small-signal voltage gain of common-drain amplifiers is always smaller than the unit, which seems to make these circuits of little use at first sight.

The small-signal input resistance is given by $r_{in} = \frac{v_{in}(t)}{i_{in}(t)} = R_{12}$ = 1.6 MΩ. This is a very large input resistance.



The small-signal output resistance is given by $r_{out} = \left.\frac{V_{test}}{I_{test}}\right|_{v_{in}(t)=0}$.



We can write: $v_{gs} = -g_m R_S v_{gs} - R_S I_{test}$, which leads to $v_{gs} = -\frac{R_S}{1+g_m R_S} I_{test}$. In addition, we have $V_{test} = -v_{gs}$.

By combining both equations, we obtain $r_{out} = \frac{R_S}{1+g_m R_S} \approx 345\ \Omega$.

Due to their high input resistance and (relatively) low output resistance (which are both very attractive features for voltage amplifiers), common-drain amplifiers can be used as the output stage of more complex circuits. However, note that a much lower output resistance can generally be obtained with a common-collector bipolar amplifier than with a common-drain MOS amplifier.